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G43M01_{uATX} (Version: 0A)

CPU: Intel Conroe, Wolfdale, Yorkfield processors in LGA775 Package.

System Chipset:

North Bridge ... Eaglelake-Q
South Bridge ... ICH10-DO

Main Memory:

Dual Channel / DDR-II * 4 (Maximum to 8GB)

On Board Device:

Clock Generator ... IDTCV183-2BPAG
Super I/O ... IT8720F
LAN ... Intel BOAZMAN (82567LM) ... GbE
HDA Codec ... ALC888S
BIOS ... SPI Flash ROM

Expansion Slots:

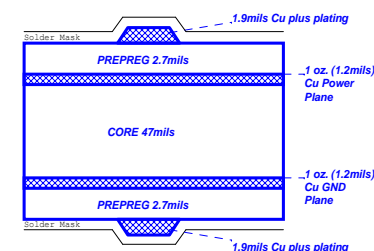
PCI EXPRESS 16X SLOT *1
PCI EXPRESS 1X SLOT * 2
PCI SLOT * 1

PWM Controller:

Controller ... NCP5392MNR2G (4Phase)
Driver ... NCP5359DR2G

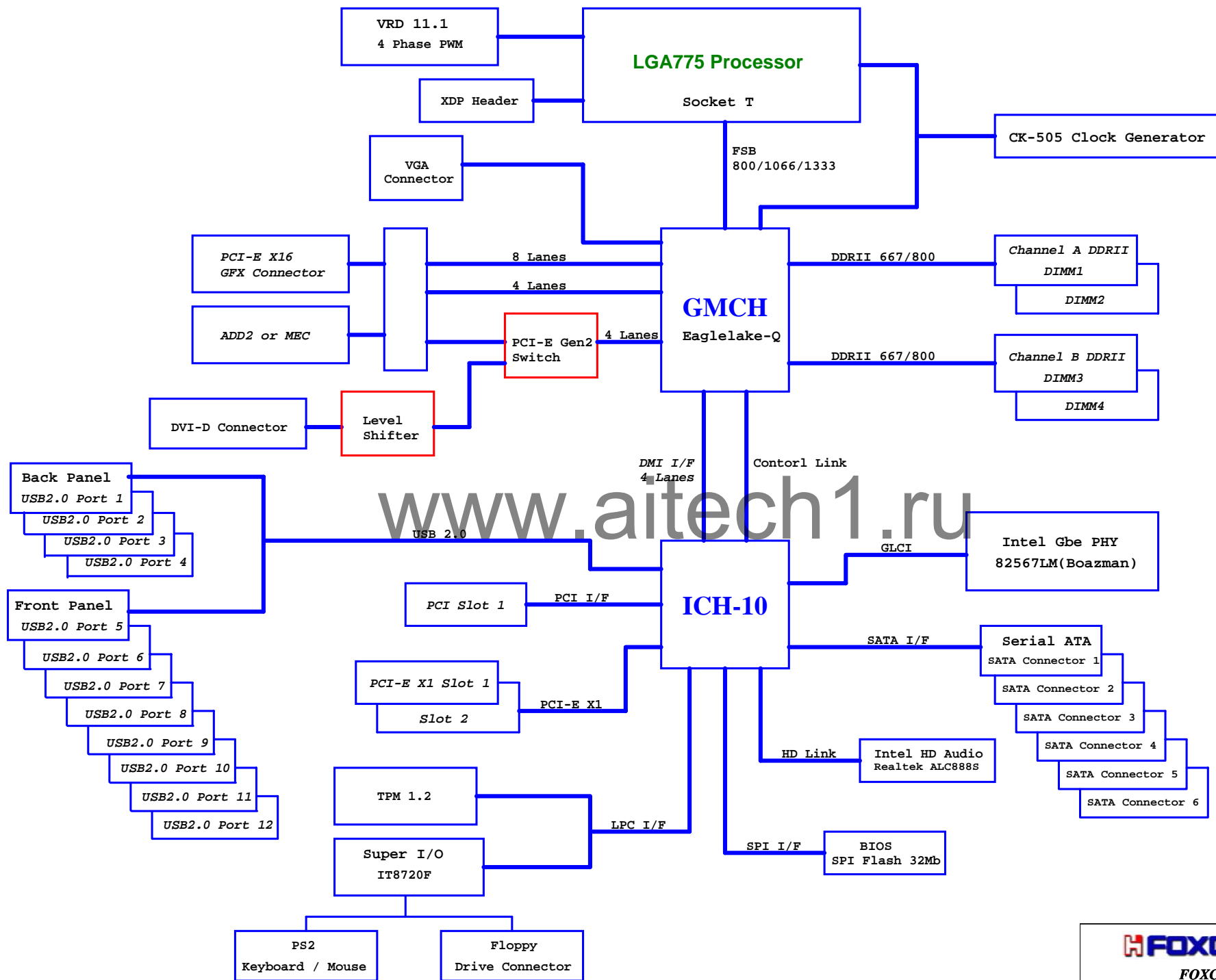
Board Stack-up

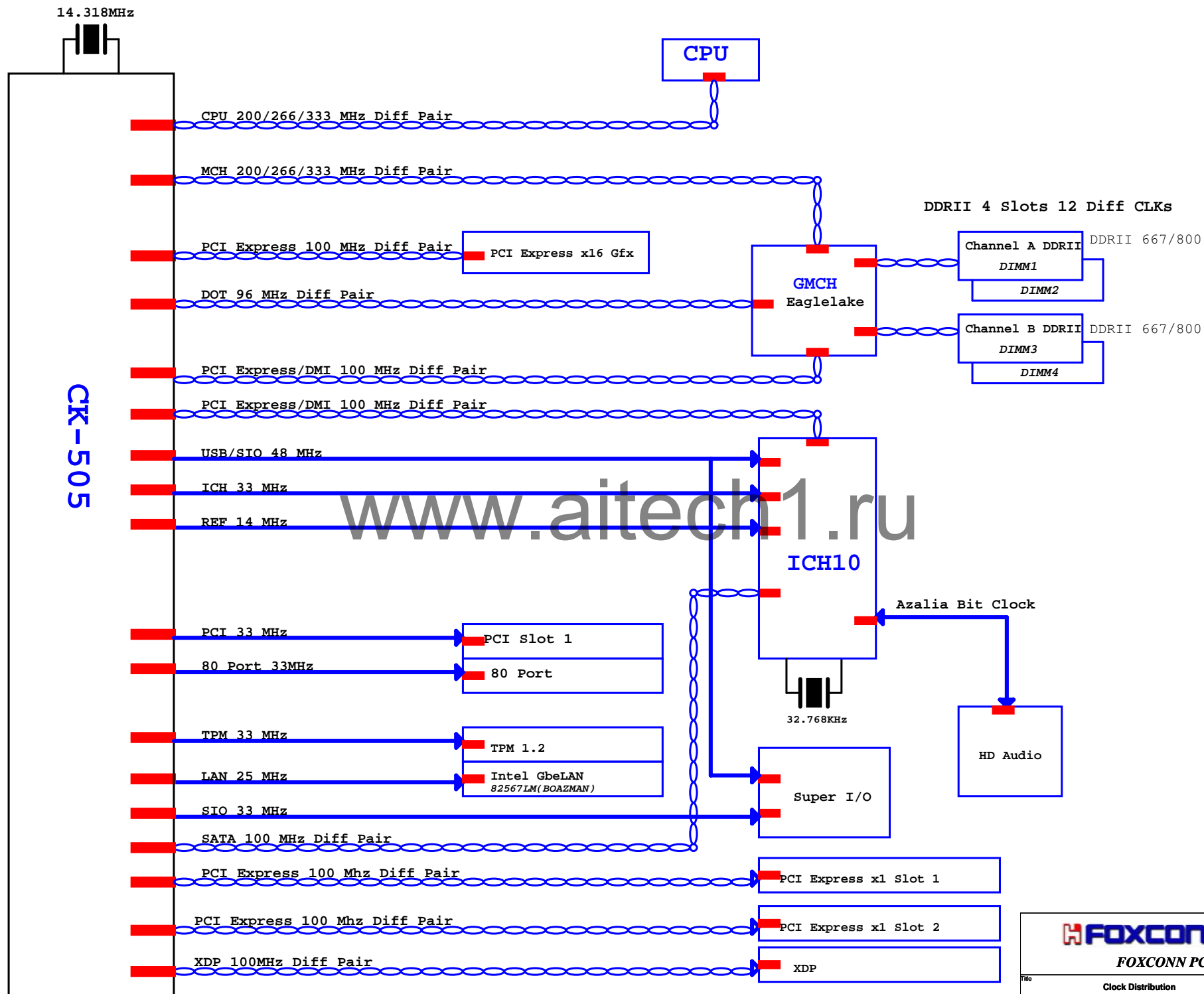
(1080 Prepreg Considerations)

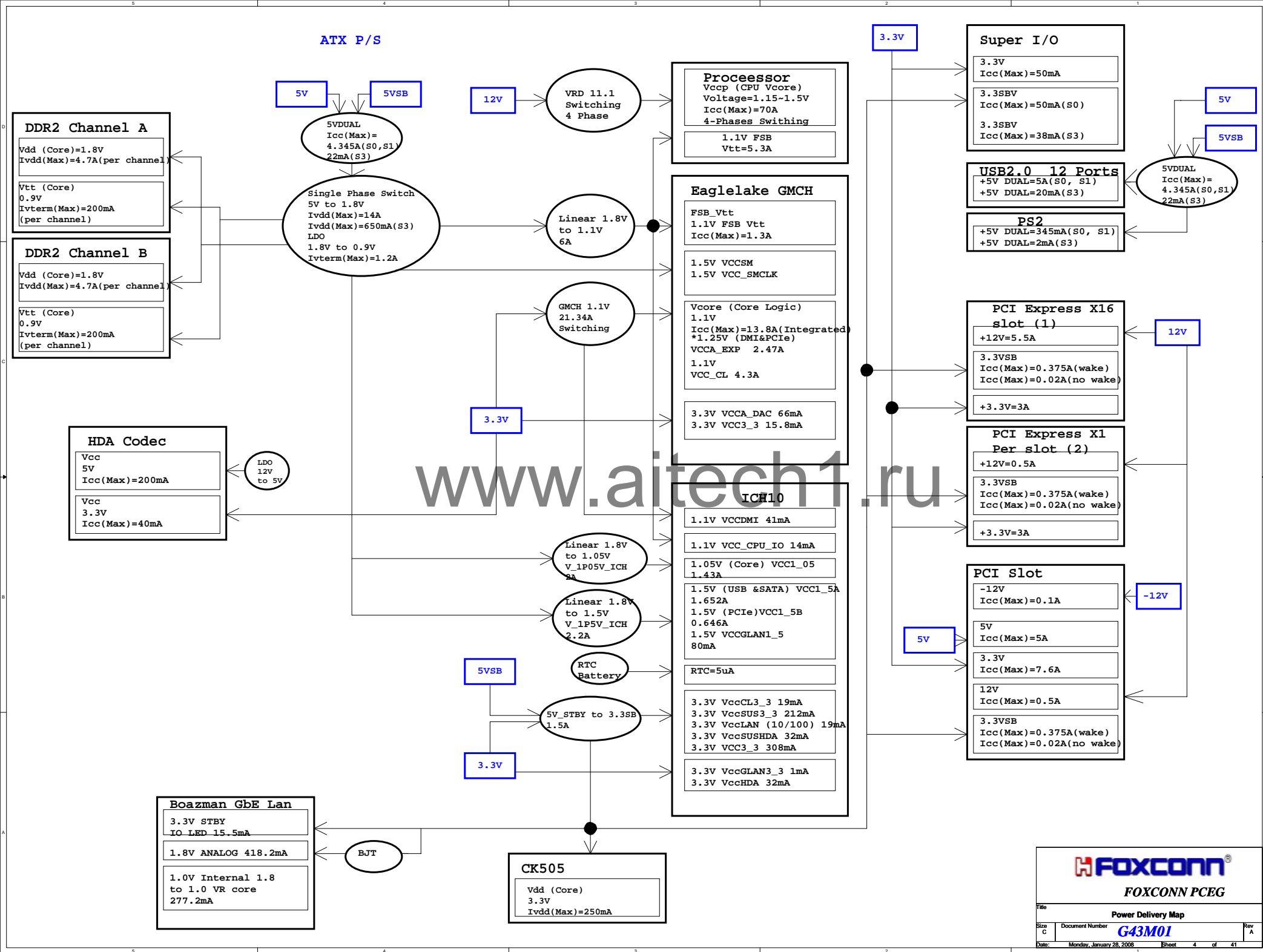


Single End 50ohm Top/Bottom : 4mils
USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
SATA - 95ohm : 15/4/8/4/15
PCIE - 95ohm : 15/4/8/4/15
DMI - 95ohm : 15/4/8/4/15

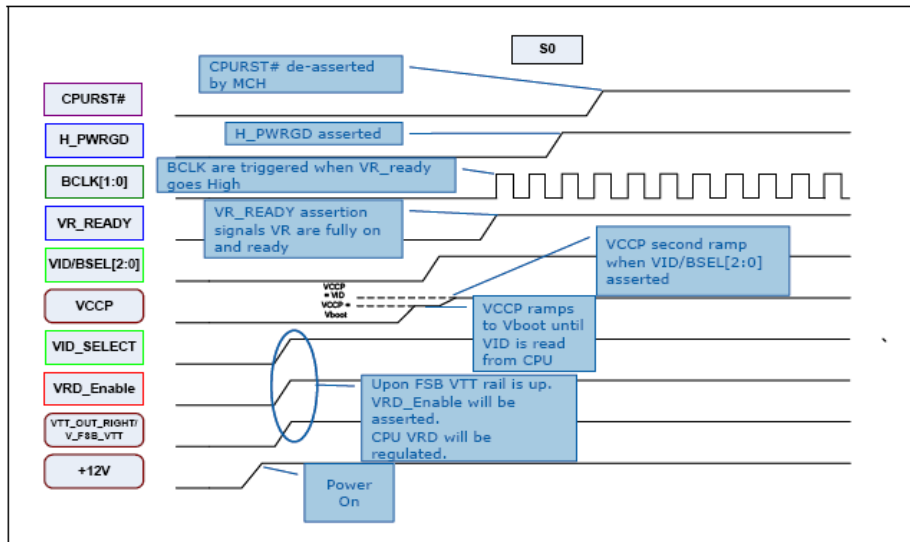
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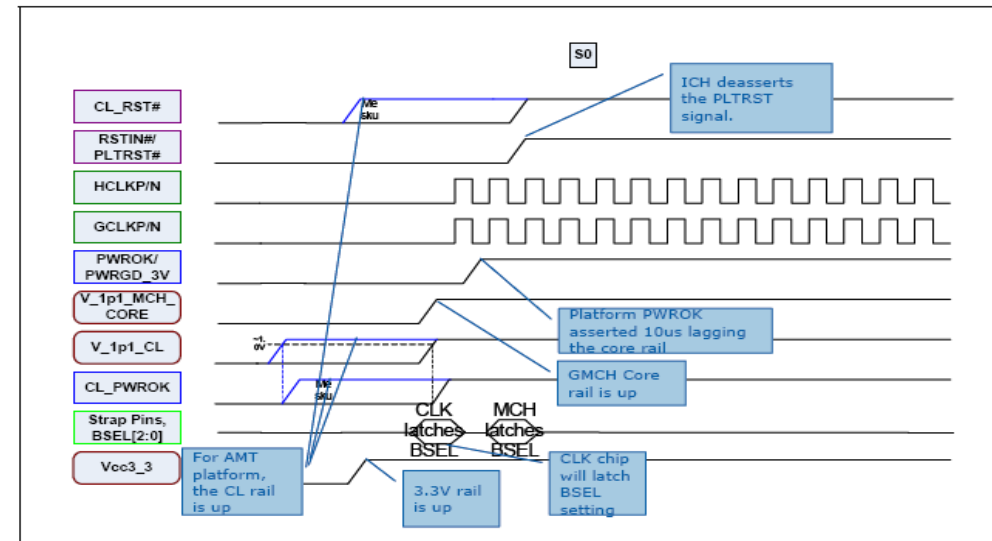




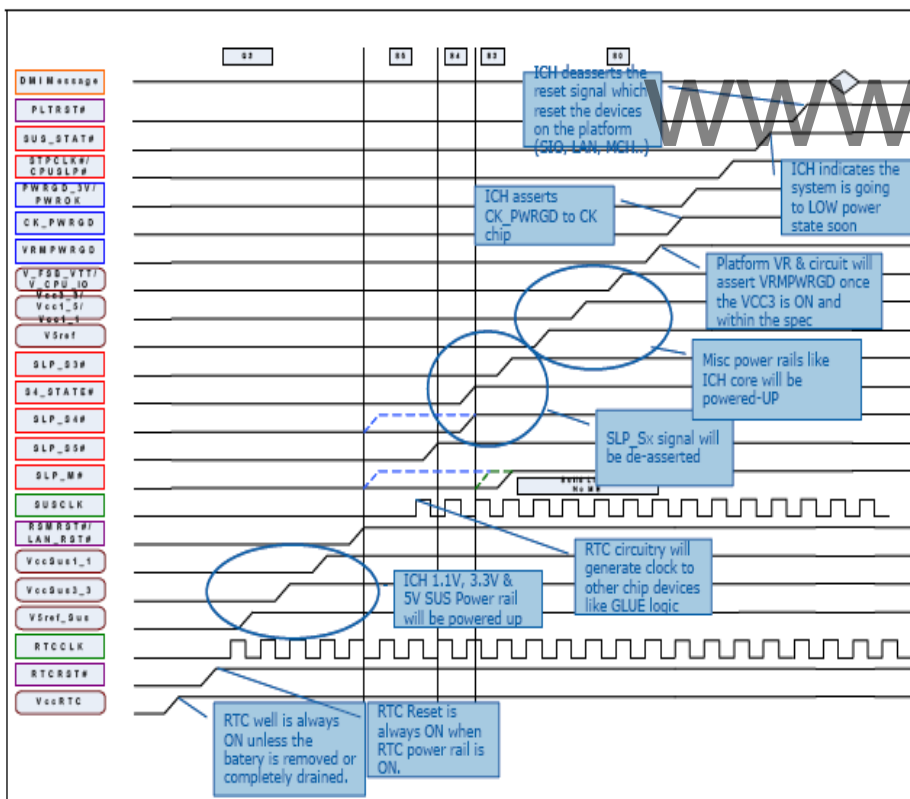
Intel® Eaglelake Platform Sequencing:- CPU VR Sequencing Diagram



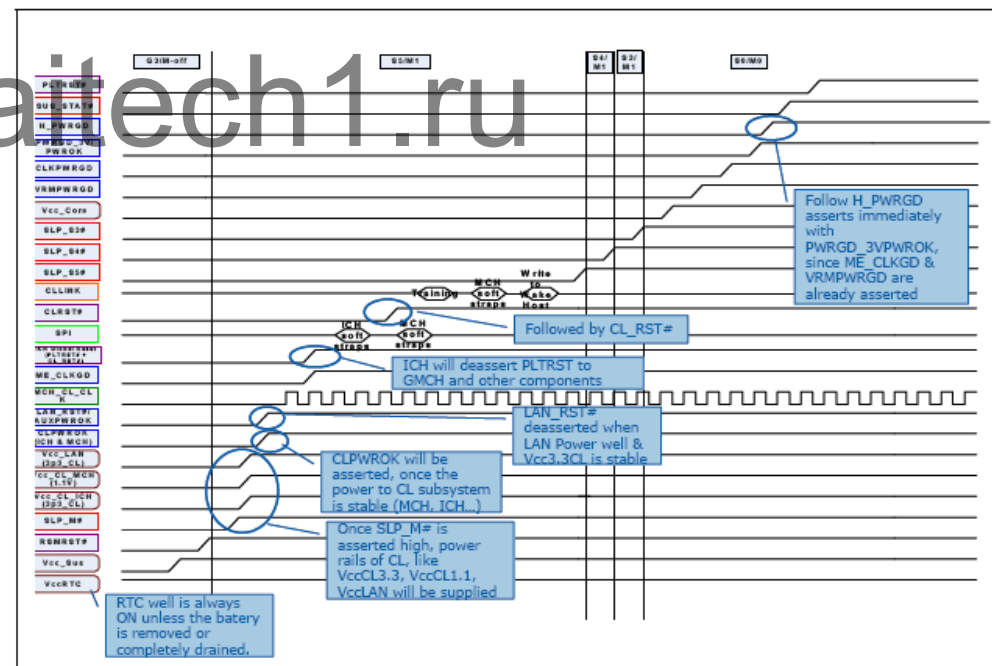
Intel® Eaglelake Platform Sequencing:- GMCH Sequencing Diagram

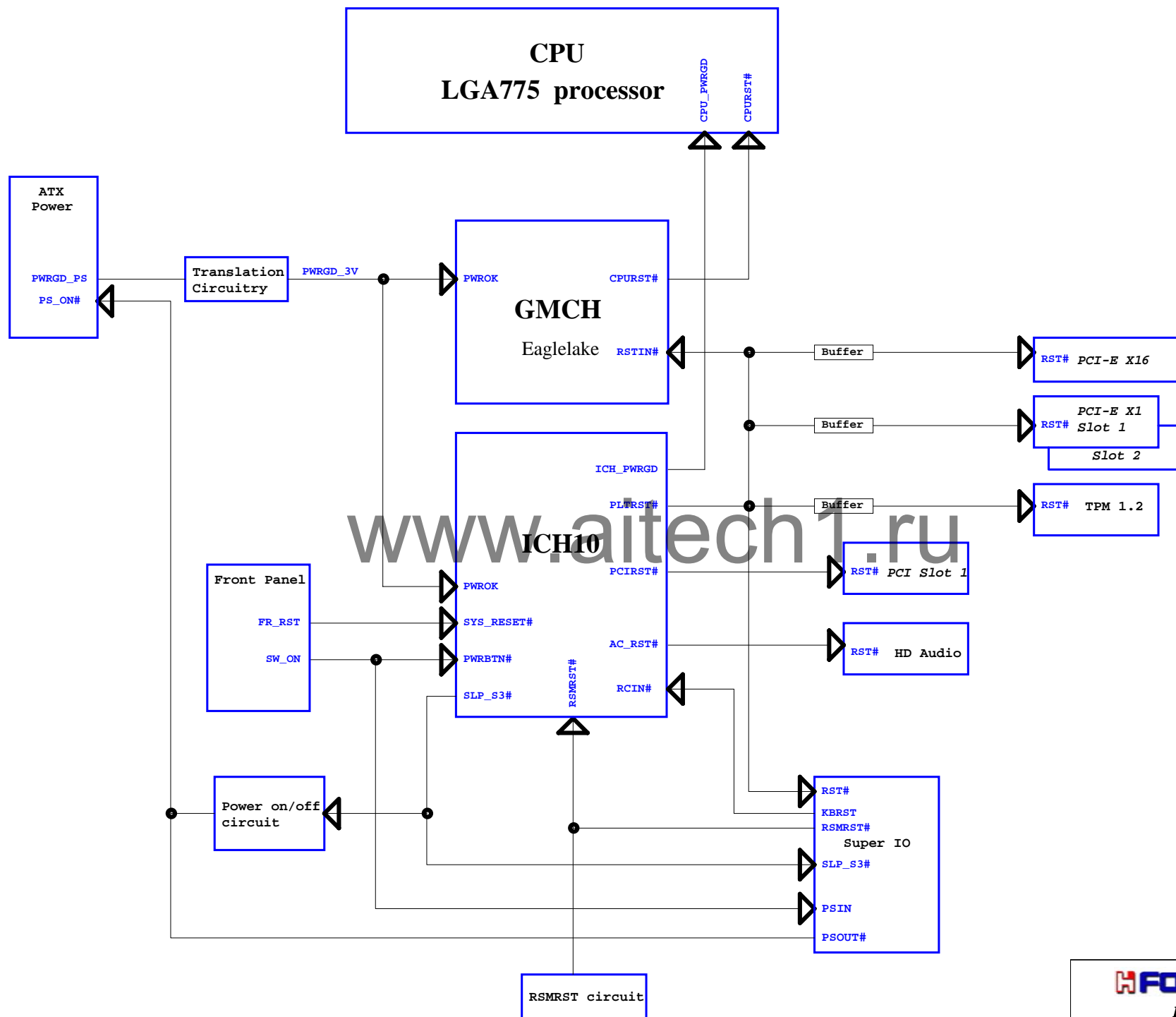


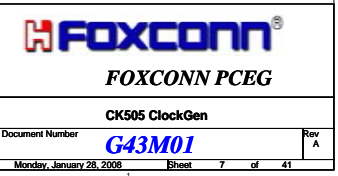
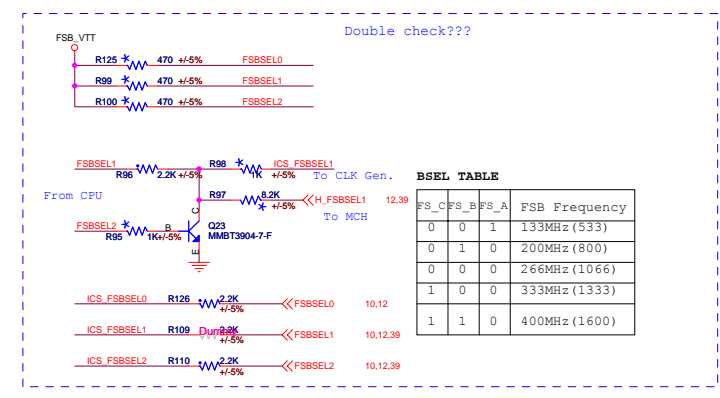
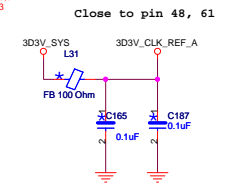
Intel® Eaglelake Platform Sequencing:- ICH10 Sequencing Diagram

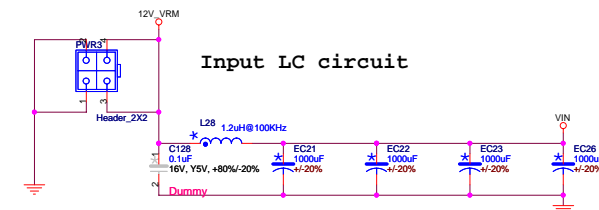
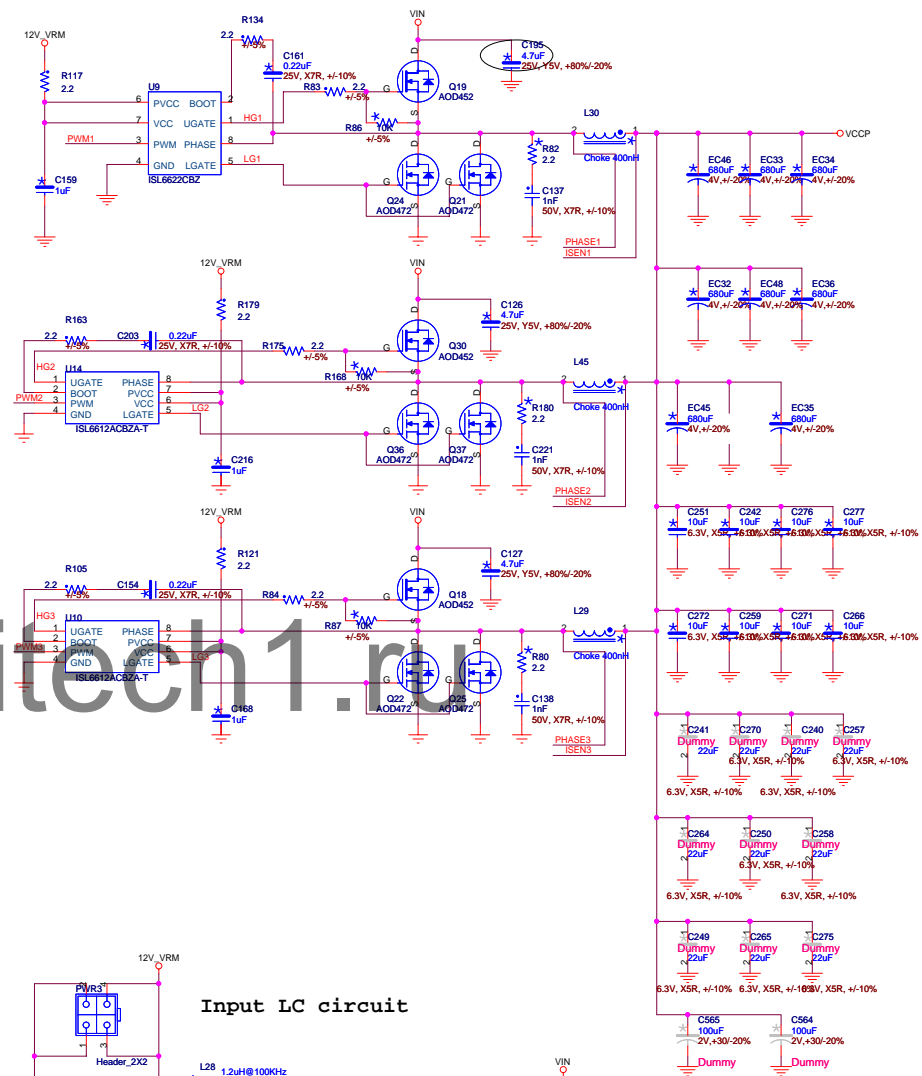


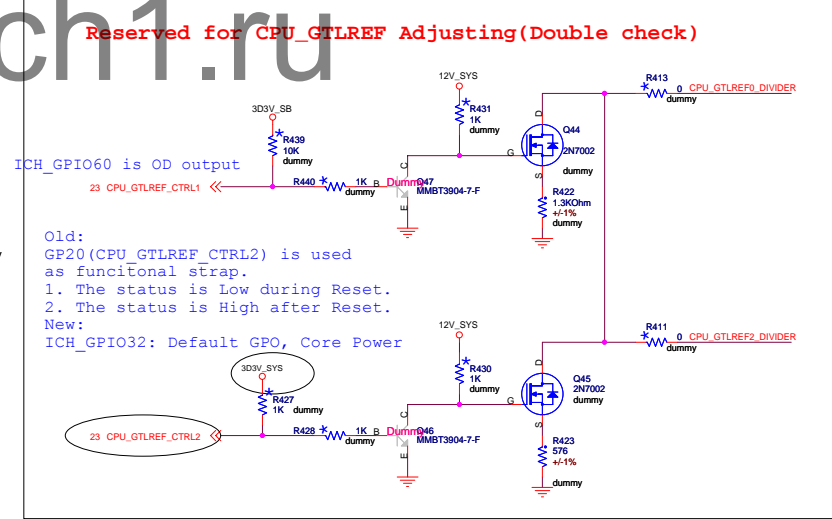
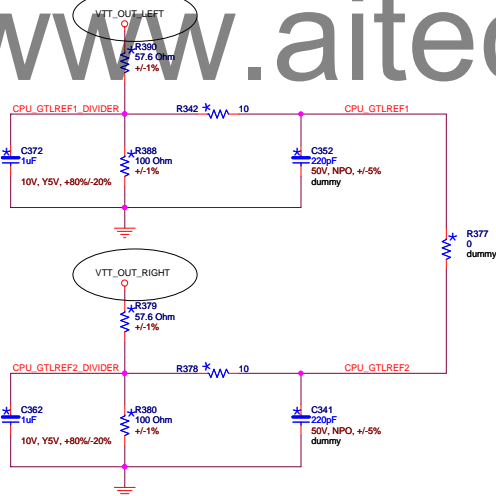
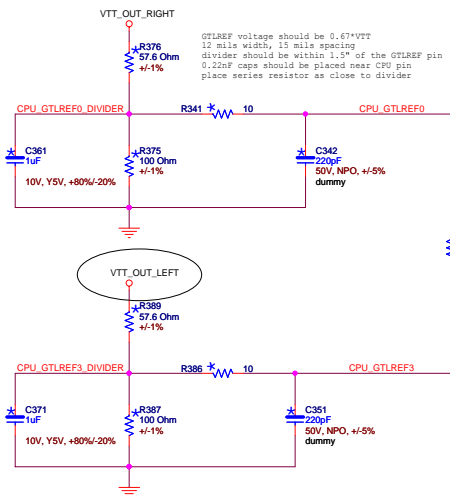
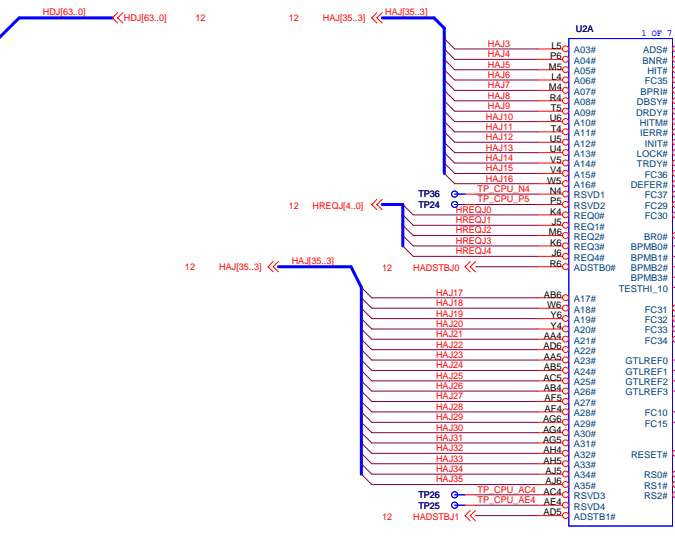
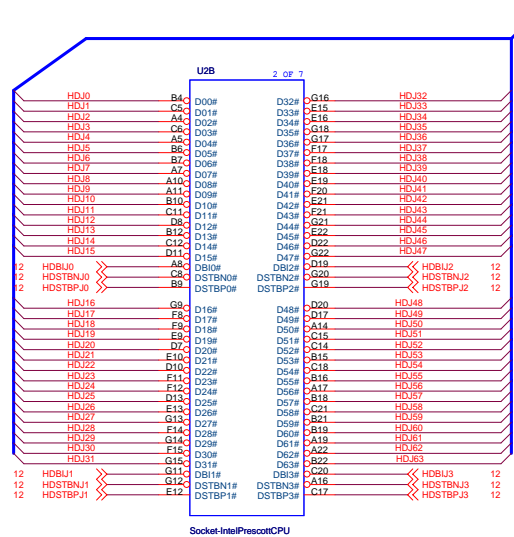
ME Platform Sequencing Diagram

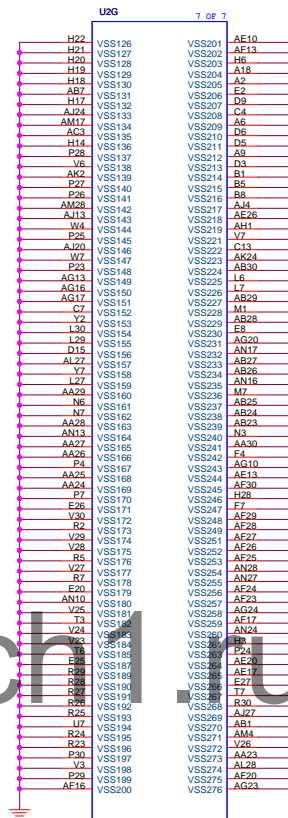
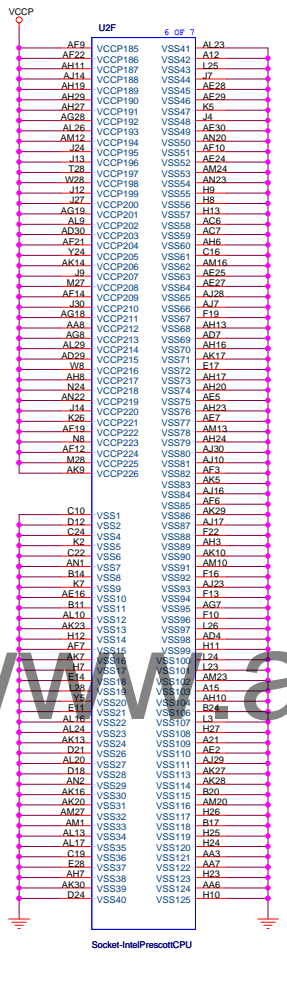
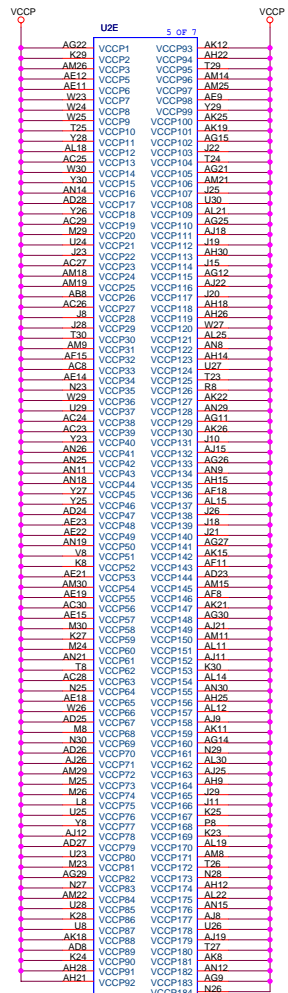


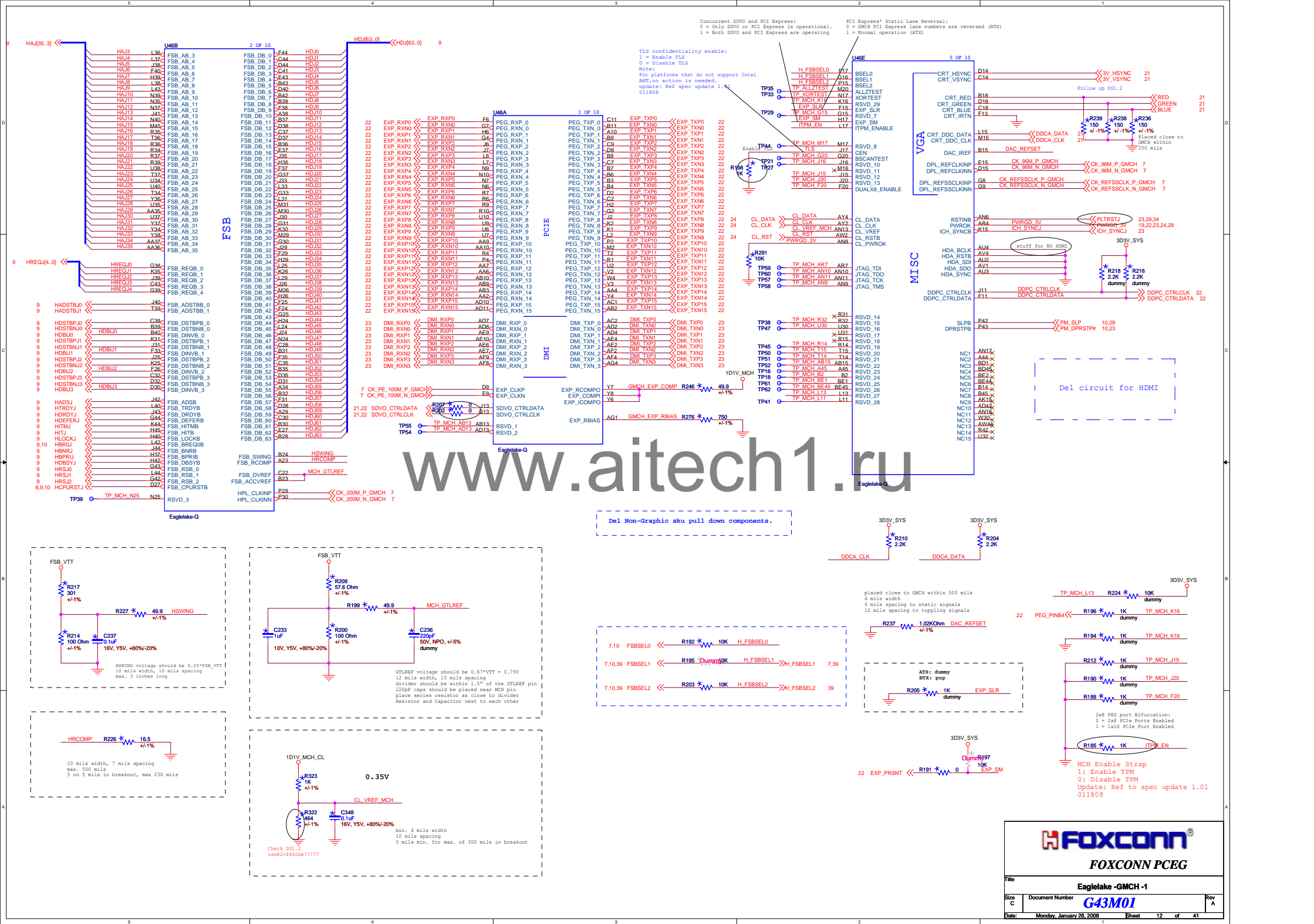


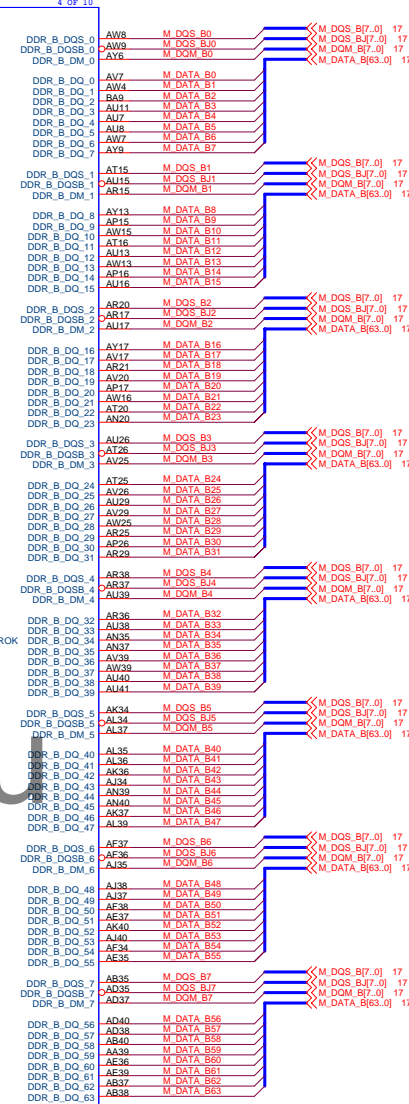
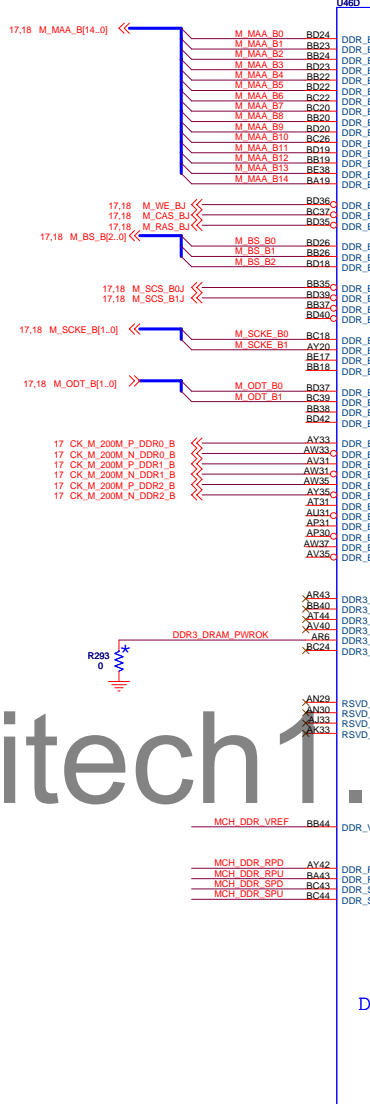
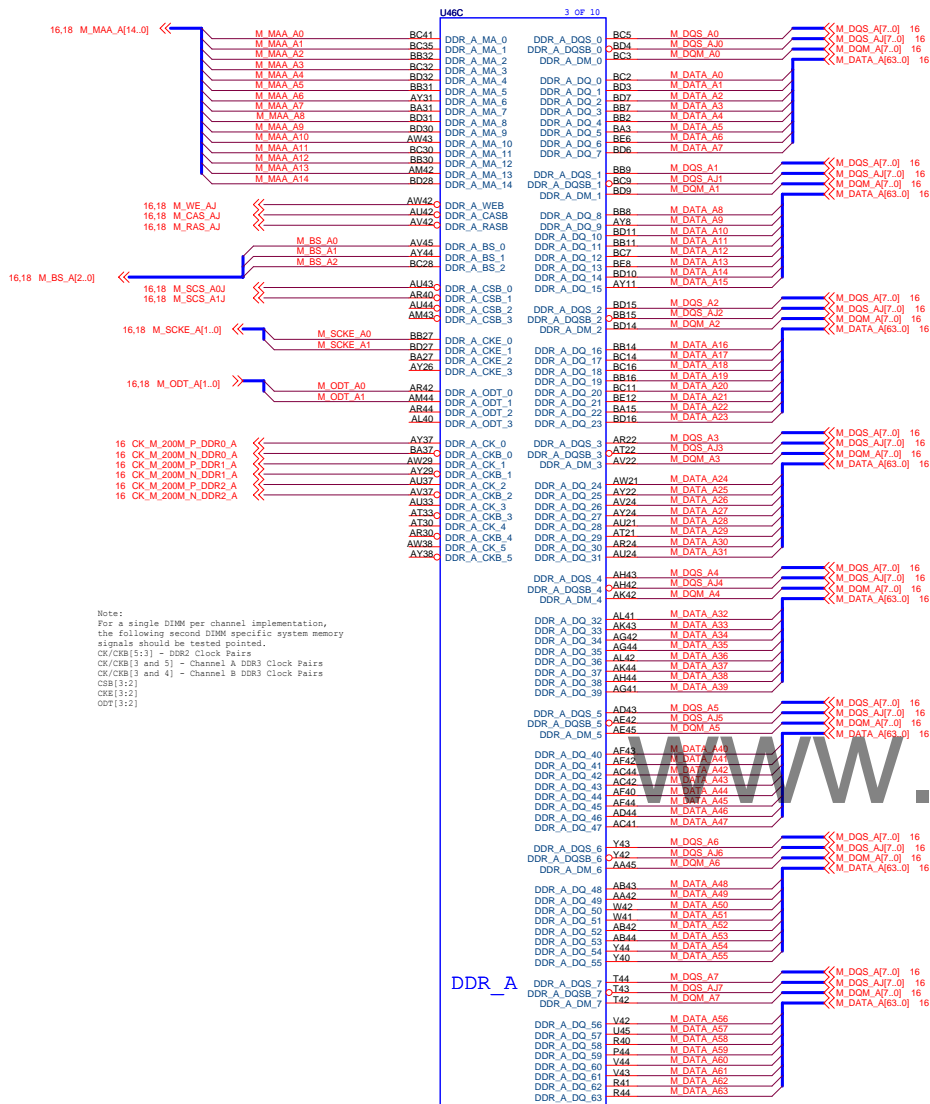




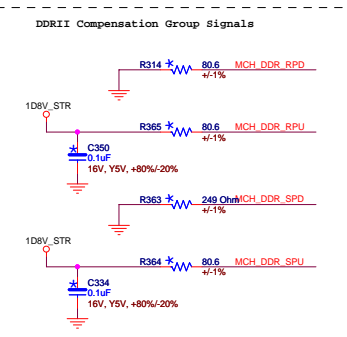
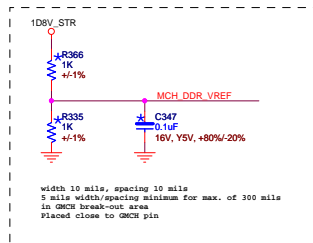


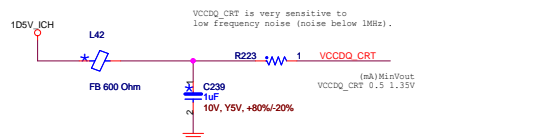




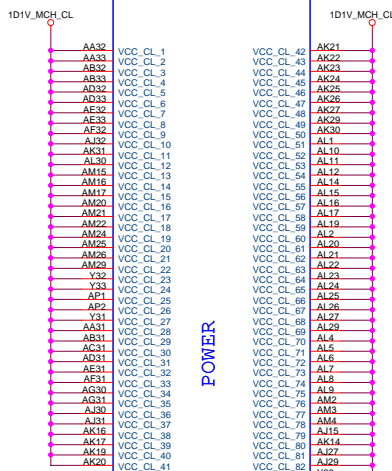
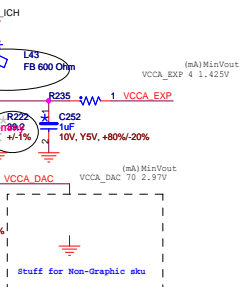


Note:
For a single DIMM per channel implementation,
the following second DIMM specific system memory
signals should be tested pointed.
CK/CDB[5:3] - DDR2 Clock Pairs
CK/CDB[3 and 5] - Channel A DDR3 Clock Pairs
CDB[3:2] and 4 - Channel B DDR3 Clock Pairs
CDB[3:2]
CDT[3:2]

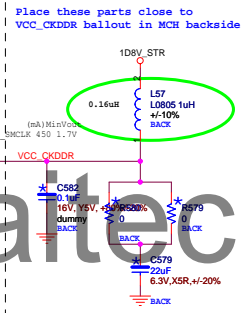




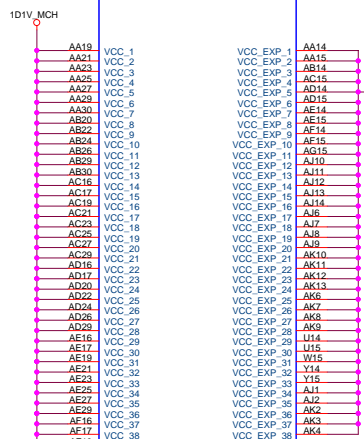
Check footprint 0603???



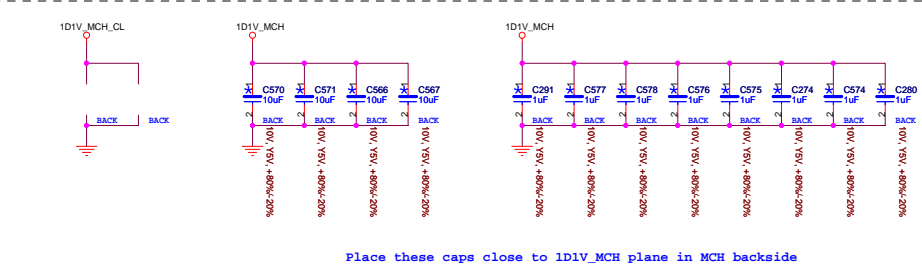
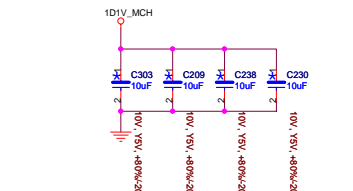
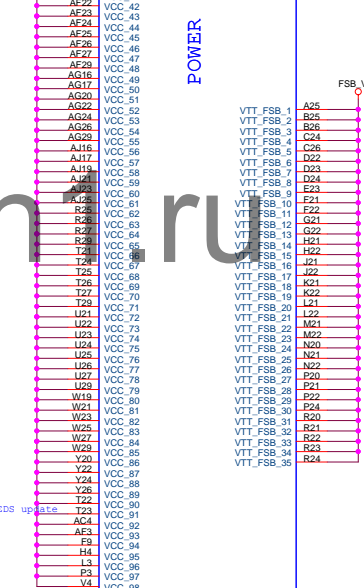
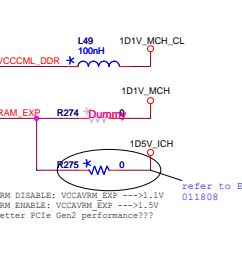
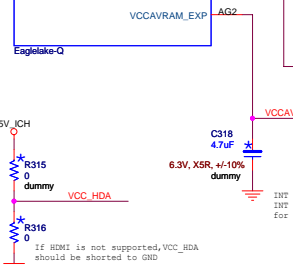
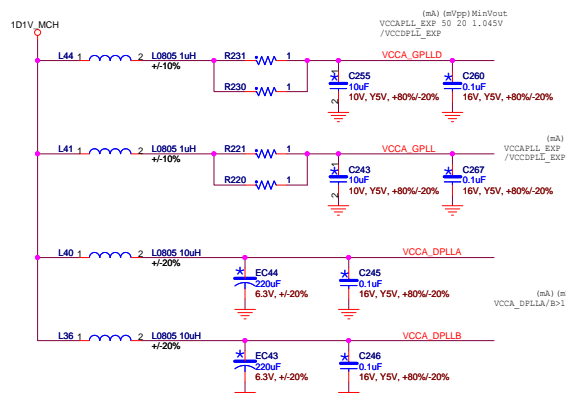
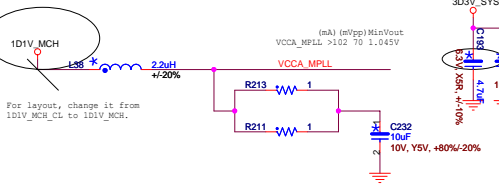
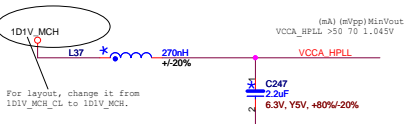
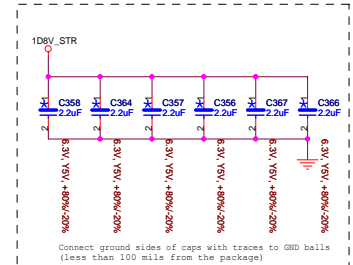
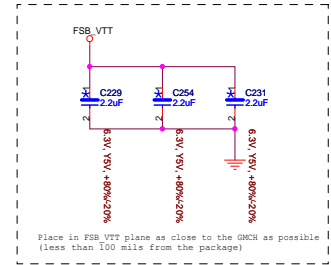
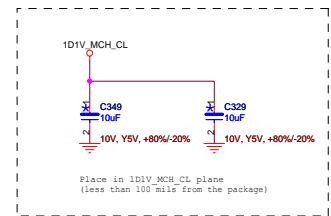
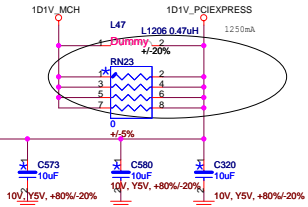
POWER



Place these parts close to VCC_KDDR ballout in MCH backside



POWER



Place these caps close to 1D1V_MCH plane in MCH backside

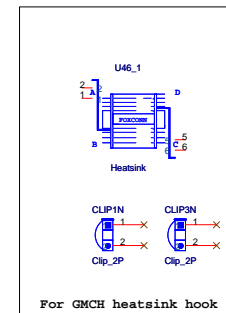
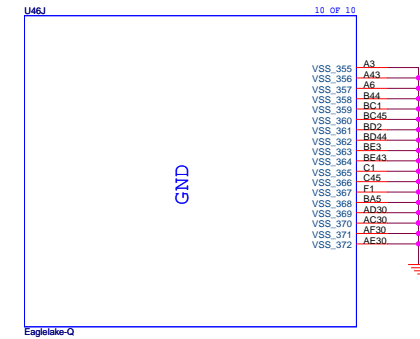
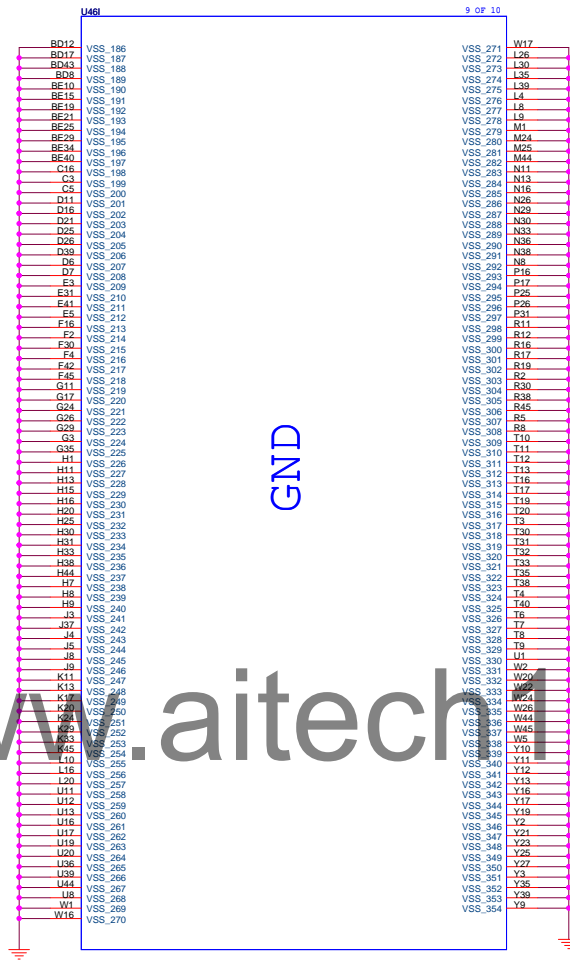
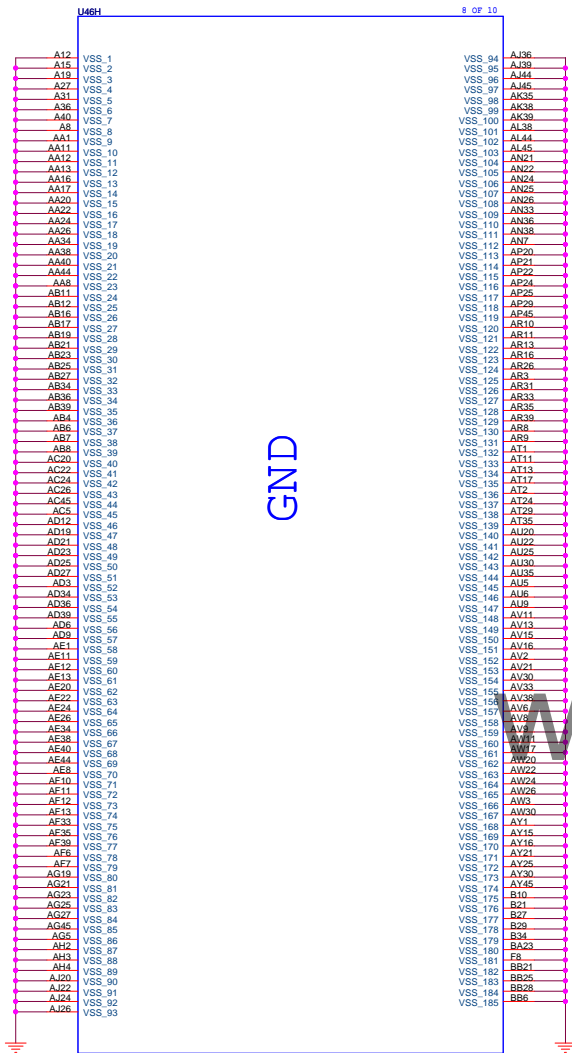
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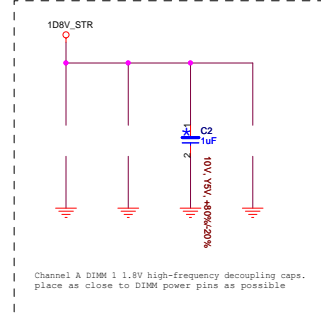
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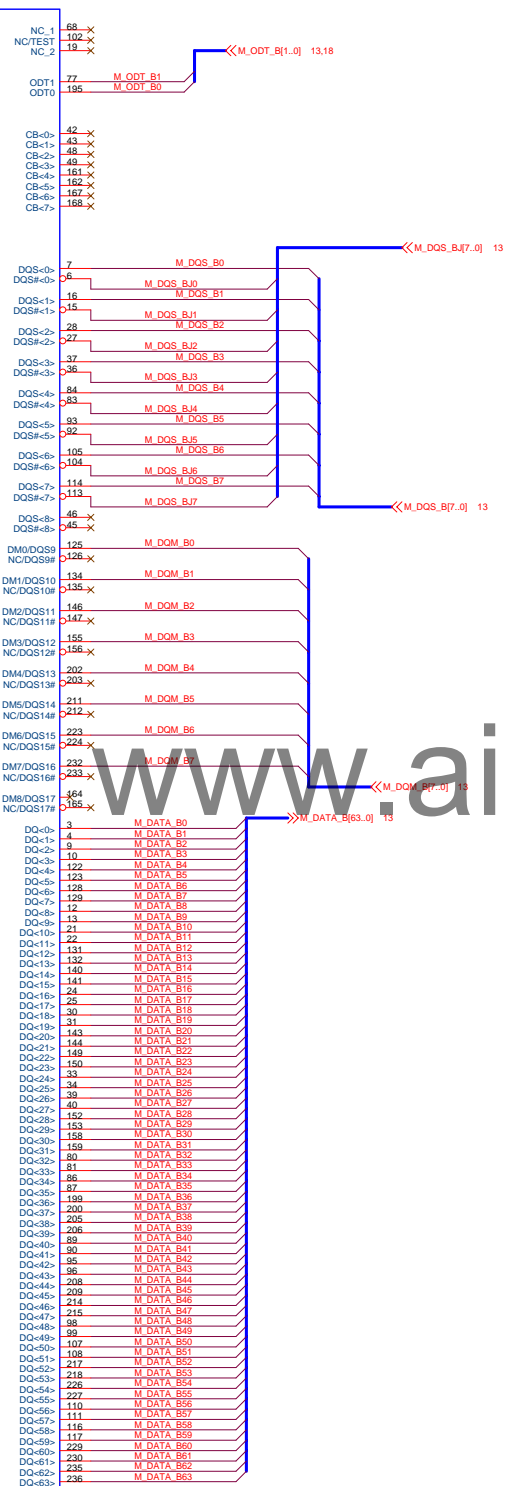
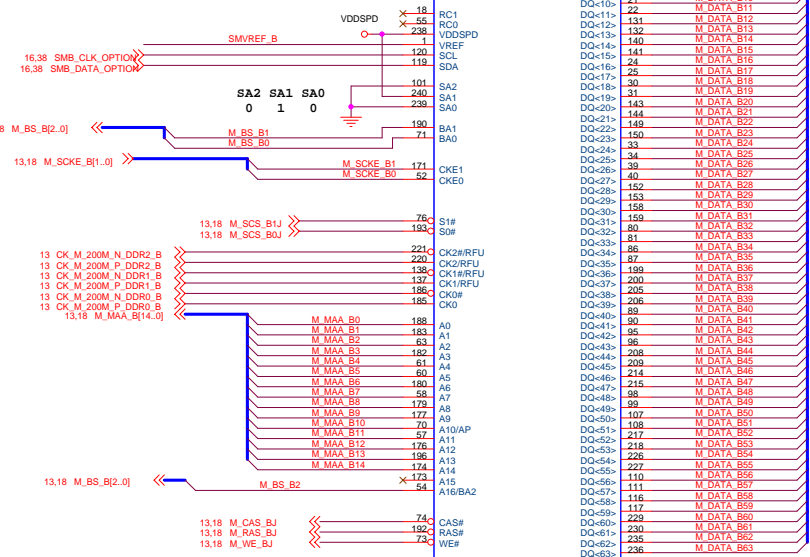
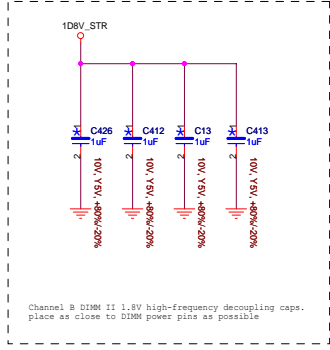
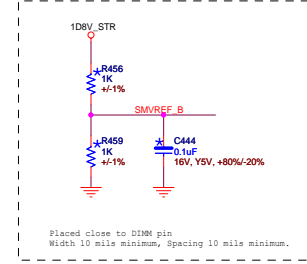
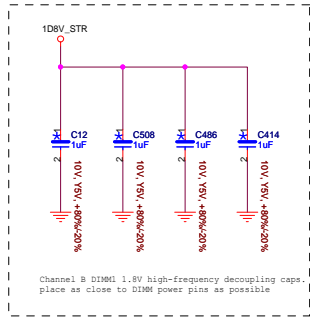
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Size: **C** Document Number: **G43M01** Rev: **A**

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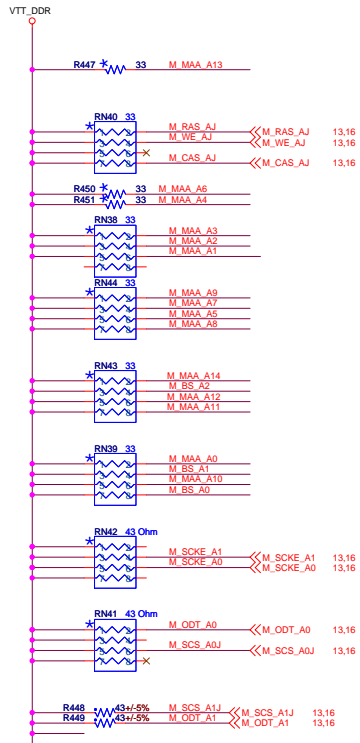




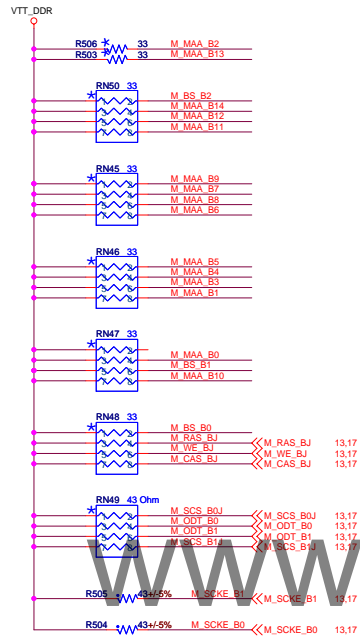


<<M_ODT_A[1..0] 13,16
 <<M_SCKE_A[1..0] 13,16
 <<M_BS_A[2..0] 13,16
 <<M_MAA_A[14..0] 13,16

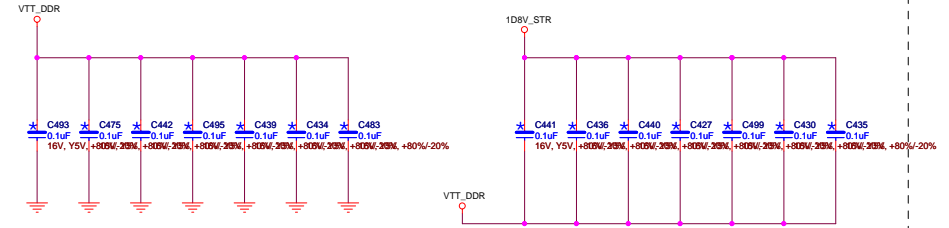
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 <<M_BS_B[2..0] 13,17
 <<M_MAA_B[14..0] 13,17
 <<M_ODT_B[1..0] 13,17



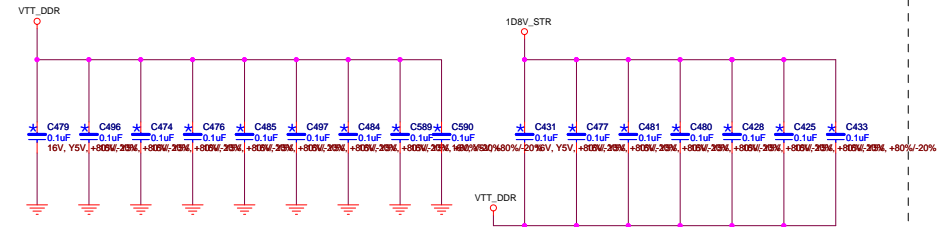
Channel A VTT_0.9V Mid Range decoupling caps.
Placed in termination Island



Channel B VTT_0.9V Mid Range decoupling caps.
Placed in termination Island



Channel A VTT_0.9V high-frequency decoupling caps.
Place as close to termination resistors as possible

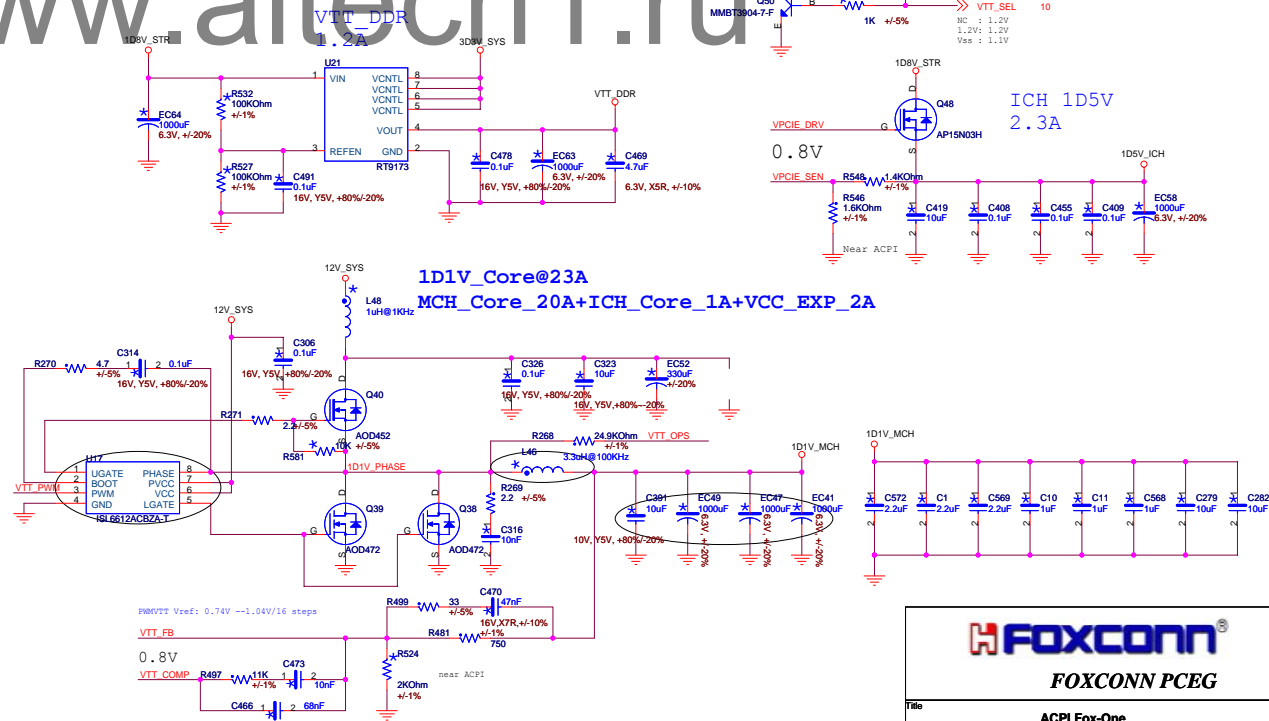
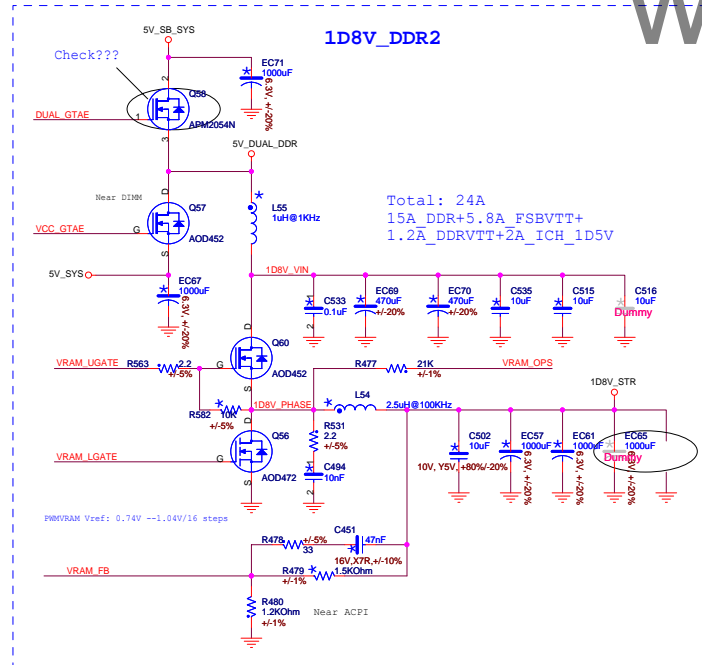
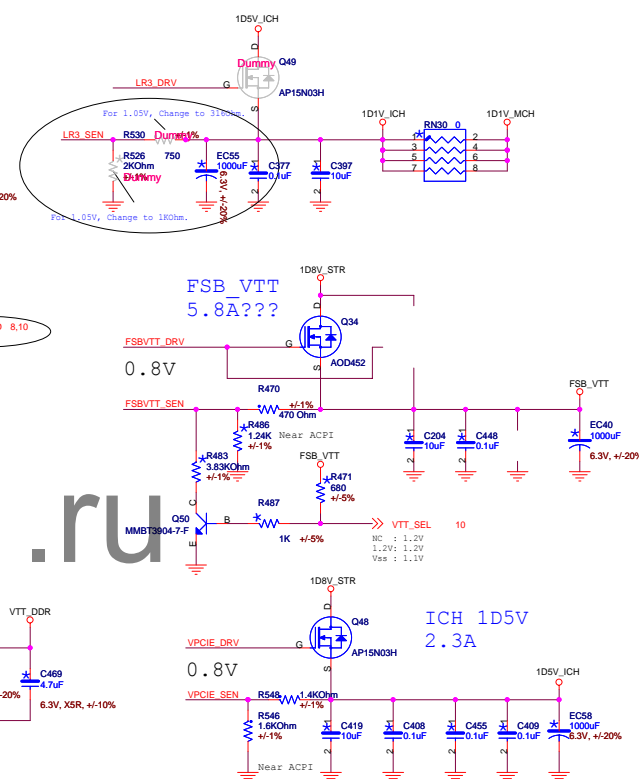
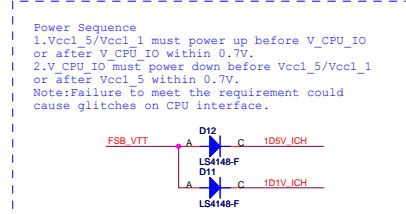
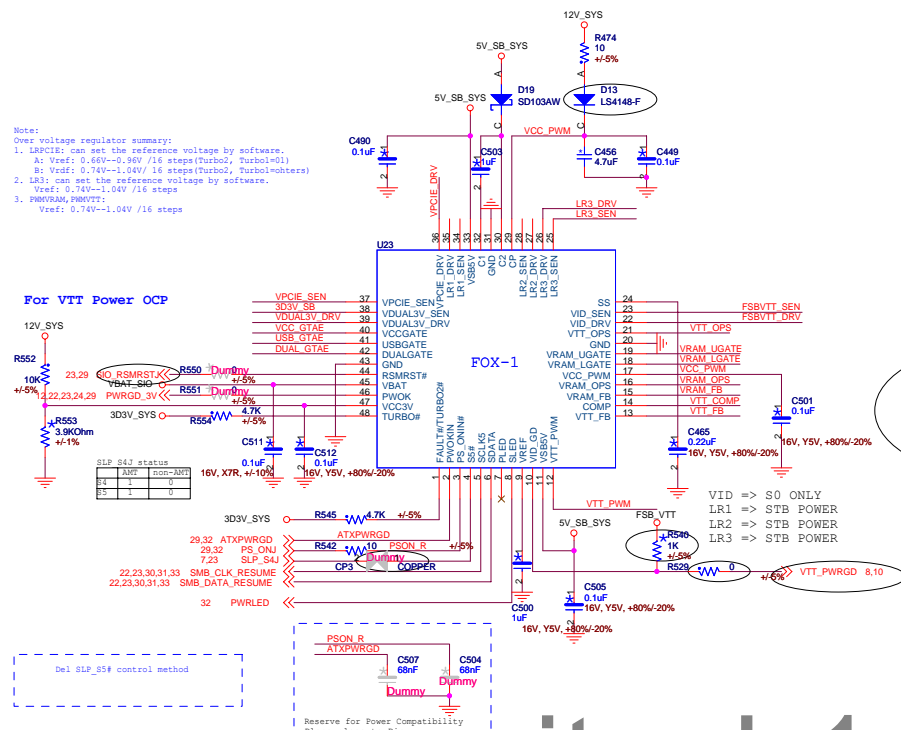
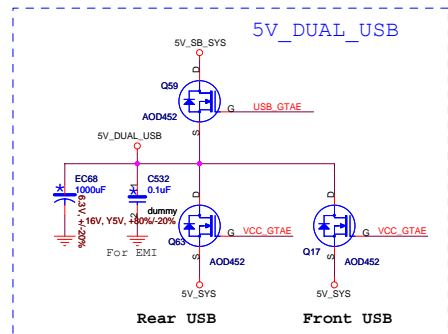
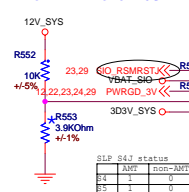
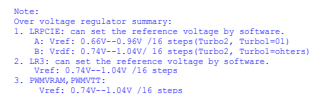


Channel B VTT_0.9V high-frequency decoupling caps.
Place as close to termination resistors as possible



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DDRII Termination		
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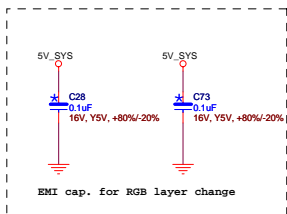


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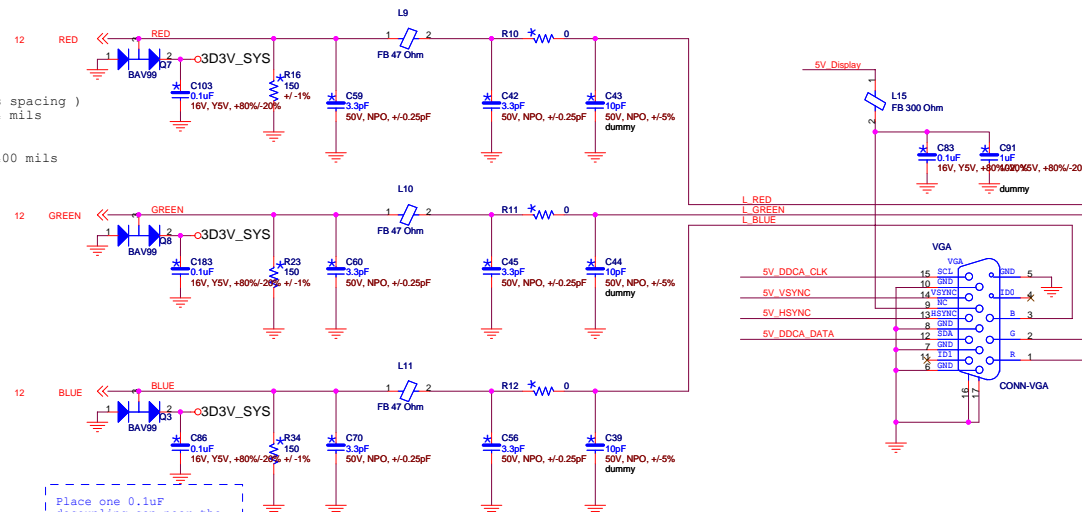
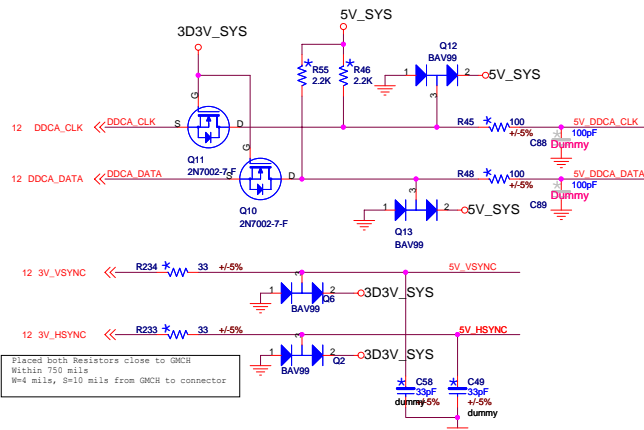


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- RGB routing
1. from GMCH to the first 150 ohm resistor: 7.5 mils (min. 6 mils spacing)
 2. from the first 150 ohm res. to the second 150 ohm resistor: 4 mils
 3. from the second 150 ohm resistor to connector: 4 mils
 4. spacing minimum 6 mils, 30 mils spacing is recommended
 5. R, G, B should be length matched to 700 mils, max. length is 8400 mils
 6. R, G, B signals should be ground referenced

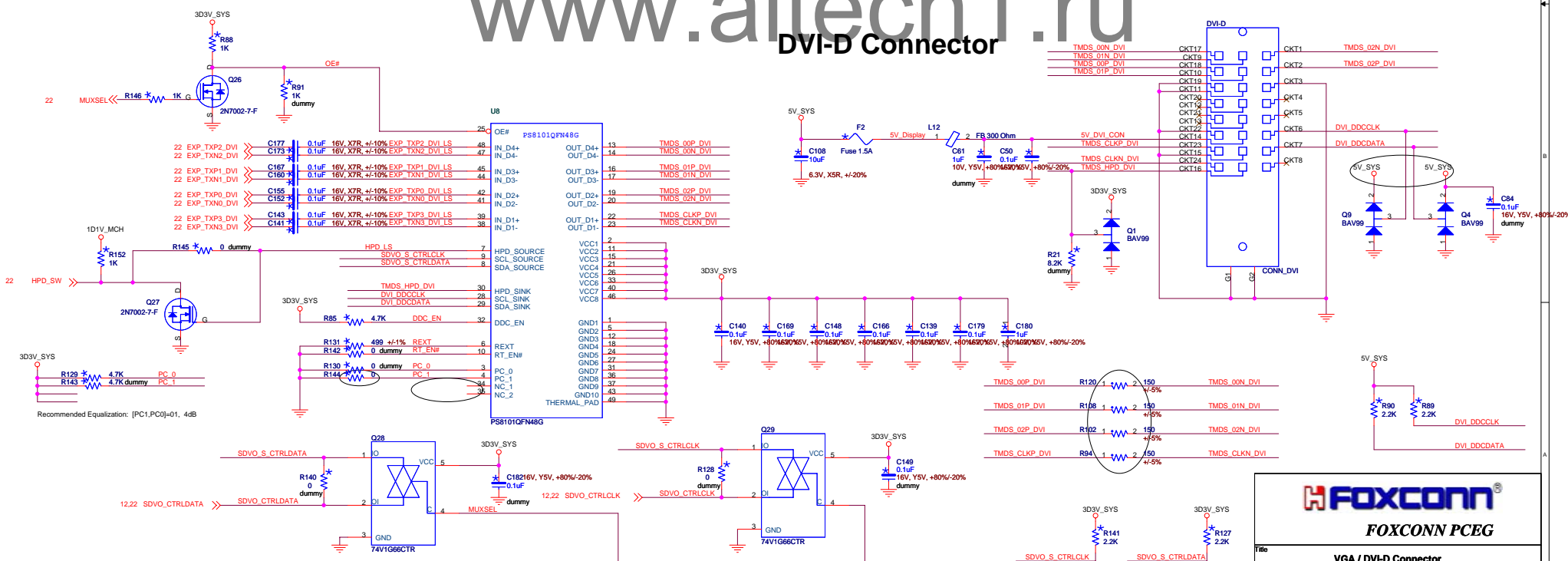


Place one 0.1uF decoupling cap near the ESD diodes

The 150 Ohm resistors near VGA connector and minimizing length to filter. The filters to VGA connector maximum distance 800 mils.

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DVI-D Connector



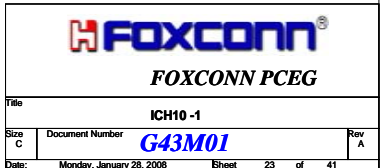
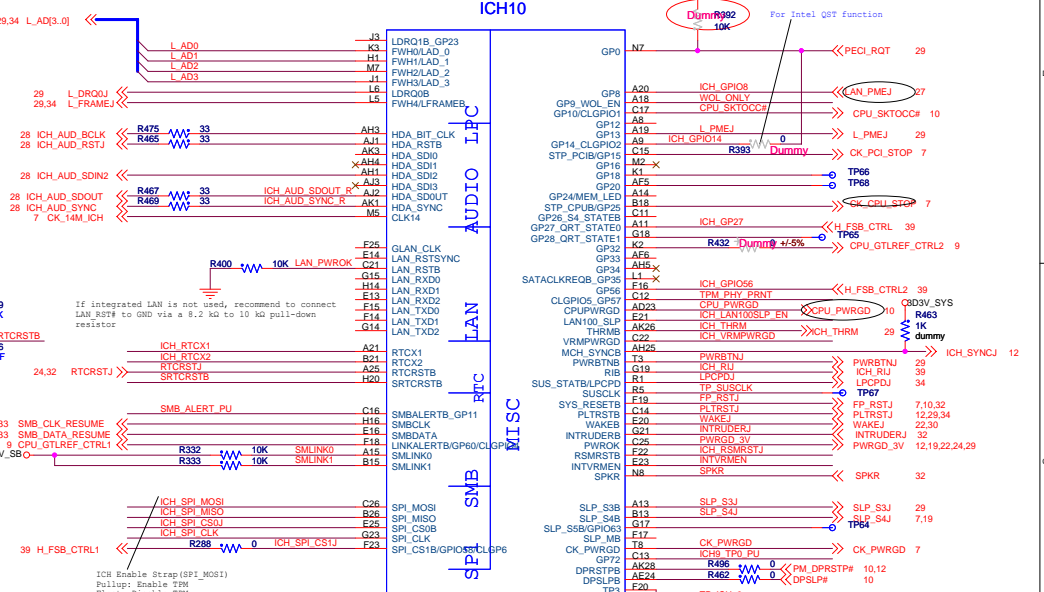
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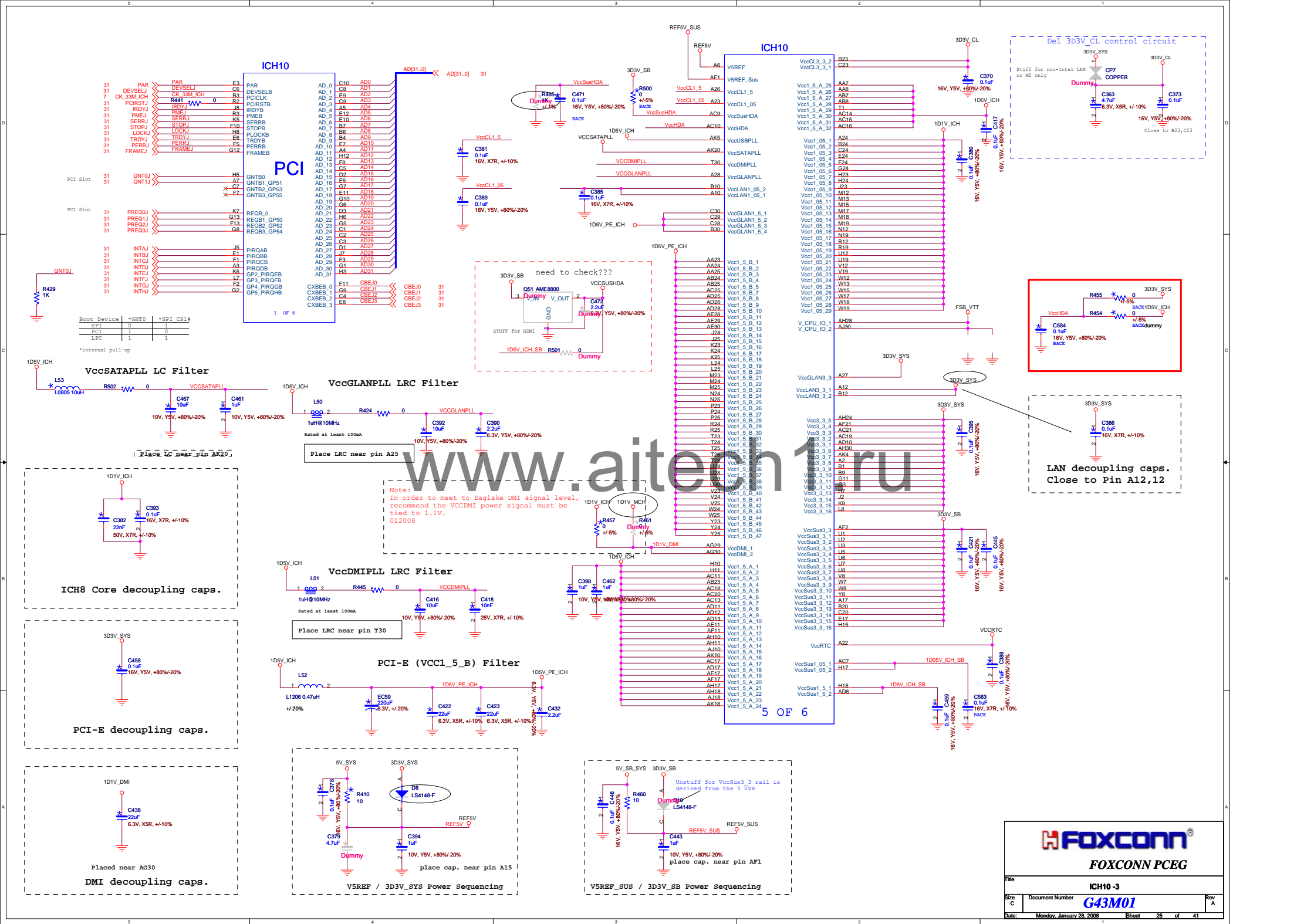
FOXCONN PCEG

File: **VGA / DVI-D Connector**

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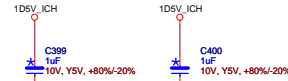




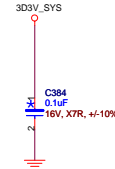
ICH10

G30	VSS_100	VSS_099	H13
G29	VSS_101	VSS_098	H19
G25	VSS_102	VSS_097	H2
F16	VSS_103	VSS_096	H22
F9	VSS_104	VSS_095	H25
F6	VSS_105	VSS_094	H26
F28	VSS_106	VSS_093	H28
F26	VSS_107	VSS_092	H5
F21	VSS_108	VSS_091	J29
F12	VSS_109	VSS_090	J30
E30	VSS_110	VSS_089	J6
E29	VSS_111	VSS_088	K26
E22	VSS_112	VSS_087	K28
E2	VSS_113	VSS_086	L23
E18	VSS_114	VSS_085	L29
E15	VSS_115	VSS_084	L30
D28	VSS_116	VSS_083	L30
D8	VSS_117	VSS_082	M14
B8	VSS_118	VSS_081	M16
B28	VSS_119	VSS_080	M26
B25	VSS_120	VSS_079	M28
B22	VSS_121	VSS_078	M6
B2	VSS_122	VSS_077	M6
B19	VSS_123	VSS_076	N13
B17	VSS_124	VSS_075	N14
B14	VSS_125	VSS_074	N15
B11	VSS_126	VSS_073	N16
AK9	VSS_127	VSS_072	N17
AK29	VSS_128	VSS_071	N23
AK2	VSS_129	VSS_070	N29
AK16	VSS_130	VSS_069	N30
AK12	VSS_131	VSS_068	P12
AJ8	VSS_132	VSS_067	P13
AJ23	VSS_133	VSS_066	P14
AJ26	VSS_134	VSS_065	P15
AJ23	VSS_135	VSS_064	P16
AJ20	VSS_136	VSS_063	P17
AJ16	VSS_137	VSS_062	P18
AJ14	VSS_138	VSS_061	P19
AJ12	VSS_139	VSS_060	P2
AH8	VSS_140	VSS_059	P28
AH6	VSS_141	VSS_058	P6
AH2	VSS_142	VSS_057	R13
AH19	VSS_143	VSS_056	R14
AH15	VSS_144	VSS_055	R15
AH13	VSS_145	VSS_054	R16
AG28	VSS_146	VSS_053	R17
AF9	VSS_147	VSS_052	R18
AF7	VSS_148	VSS_051	R23
AF29	VSS_149	VSS_050	R29
AF26	VSS_150	VSS_049	R30
AF23	VSS_151	VSS_048	R8
AF20	VSS_152	VSS_047	T12
AF15	VSS_153	VSS_046	T13
AF13	VSS_154	VSS_045	T14
AE9	VSS_155	VSS_044	T15
AE8	VSS_156	VSS_043	T16
AE6	VSS_157	VSS_042	T17
AE5	VSS_158	VSS_041	T18
AE26	VSS_159	VSS_040	T19
AE19	VSS_160	VSS_039	T2
AE18	VSS_161	VSS_038	T29
AE16	VSS_162	VSS_037	T5
AE15	VSS_163	VSS_036	U13
AE14	VSS_164	VSS_035	U14
AE13	VSS_165	VSS_034	U15
AE12	VSS_166	VSS_033	U16
AE10	VSS_167	VSS_032	U17
AD7	VSS_168	VSS_031	U18
AD3	VSS_169	VSS_030	U23
AD22	VSS_170	VSS_029	U13
AD19	VSS_171	VSS_028	V14
AD18	VSS_172	VSS_027	V15
AD16	VSS_173	VSS_026	V16
AD15	VSS_174	VSS_025	V17
AD14	VSS_175	VSS_024	V18
AD13	VSS_176	VSS_023	V26
AD12	VSS_177	VSS_022	V28
AD11	VSS_178	VSS_021	V3
AD10	VSS_179	VSS_020	V7
AC8	VSS_180	VSS_019	W1
AC5	VSS_181	VSS_018	W14
AC30	VSS_182	VSS_017	W16
AC29	VSS_183	VSS_016	W23
AC24	VSS_184	VSS_015	W29
AC12	VSS_185	VSS_014	W30
AC1	VSS_186	VSS_013	W5
AB3	VSS_187	VSS_012	W6
AB28	VSS_188	VSS_011	Y26
AB26	VSS_189	VSS_010	Y28
AA6	VSS_190	VSS_009	Y3
AA5	VSS_191	VSS_008	Y7
AK27	VSS_192	VSS_007	AA30
AK29	VSS_193	VSS_006	AA29
AA4	VSS_194	VSS_005	AA1
AF3	VSS_195	VSS_004	A30
B27	VSS_196	VSS_003	A1
	VSS_197	VSS_002	
	VSS_198	VSS_001	

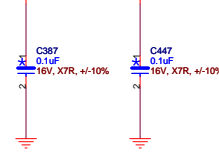
6 OF 6



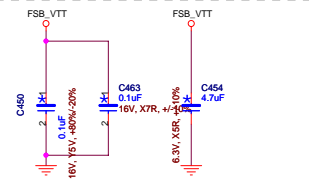
SATA decoupling caps.



PCI decoupling caps.

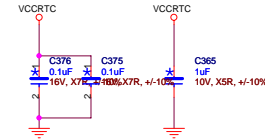


Audio decoupling caps.



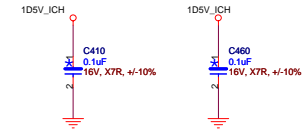
Placed near AH28 and AJ30

CPU decoupling caps.



Placed near A22

RTC decoupling caps.



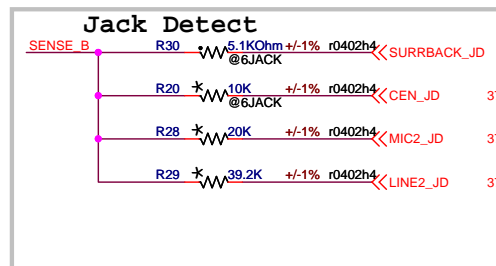
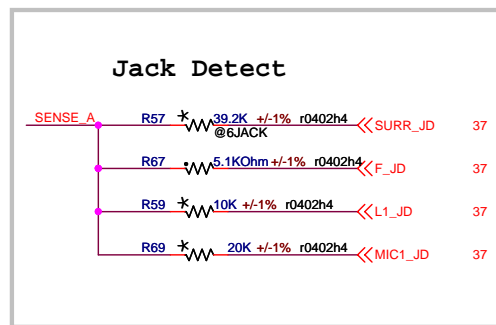
USB decoupling caps.

Del PLTRST# and PCIRST# buffer
Use SIO PCIRST# buffer

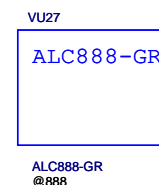
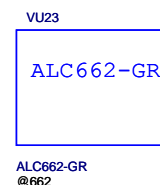
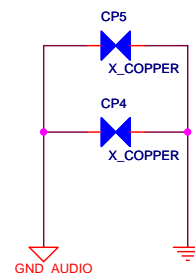
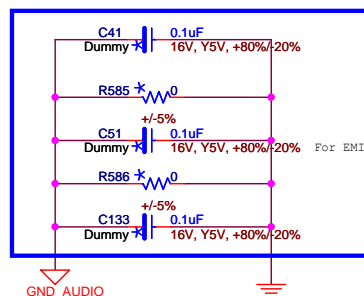
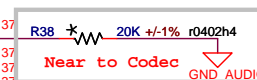
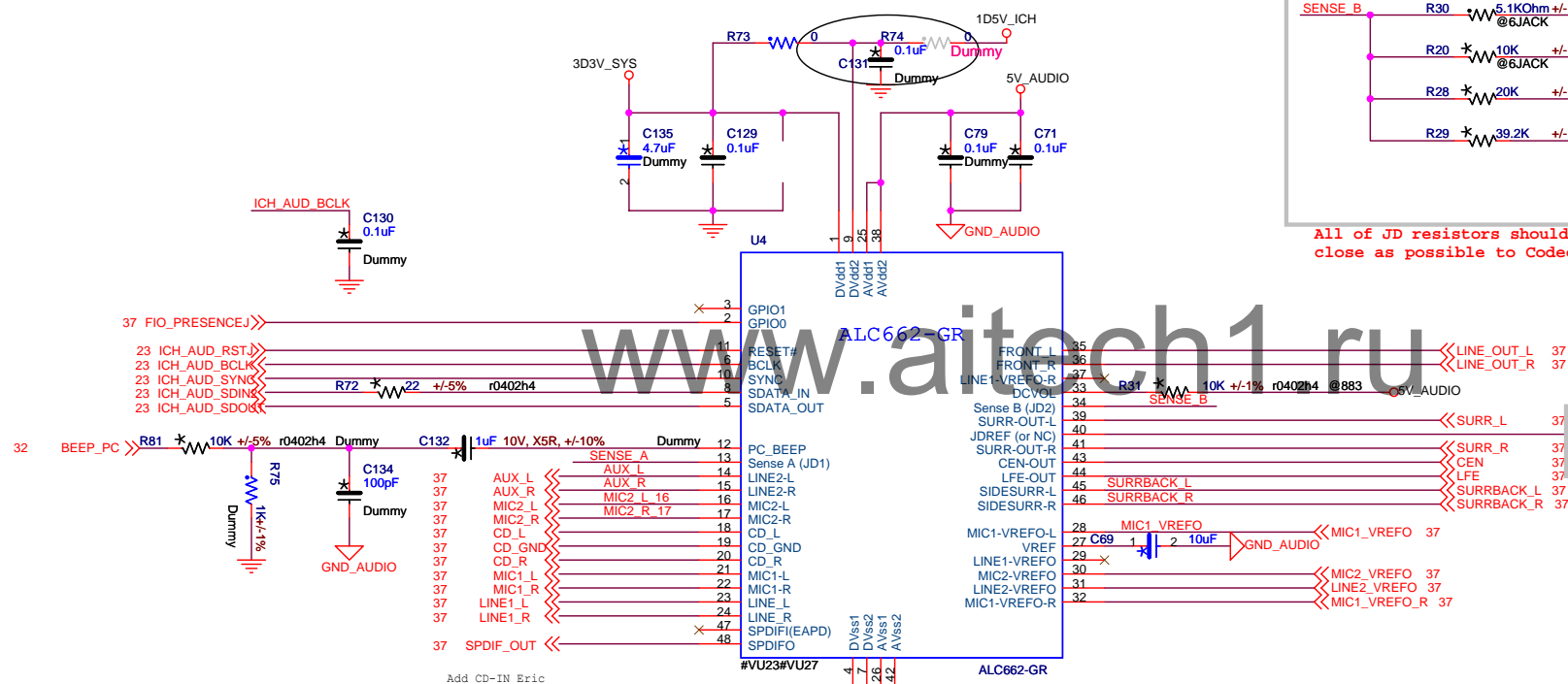
FOXCONN

FOXCONN PCEG

File		ICH10 -4	
Size	Document Number	G43M01	
C		Date	Monday, January 28, 2006
		Sheet	26 of 41
		Rev	A



All of JD resistors should be placed as close as possible to Codec.



FOXCONN PCEG

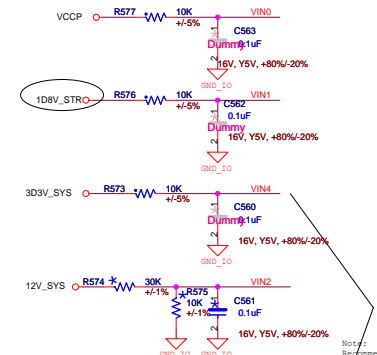
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Size	Document Number	<i>G43M01</i>
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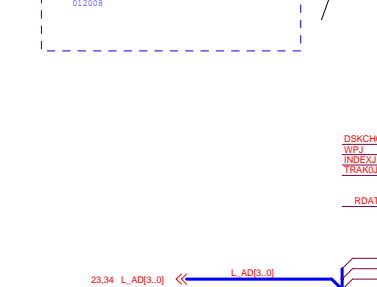
Date: Monday, January 28, 2008 Sheet 28 of 41

If without use these pins, Please pull-up to VCC.
Don't let it floating

- 1.Pin 30:RESETCON#
- 2.Pin 95:VIN3/ATXPG
- 3.Pin 71:SUSB#
- 4..Power On Strapping Options pin
- 5.Please don't remove the pull-up resistor (R108) of pin38/LDRQ#.
- 6.Please don't remove any components in the VINx circuits and the FANx control circuits.
- 7.Please don't change the sequence of VIN0-VIN6.
- 8.If without use these pins,please pull-up to VCC, Don't let it floating ,pin 3, pin 30, pin 38, pin 46, pin 95, pin 122, pin 124, pin 126.

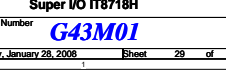
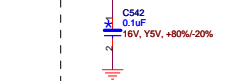
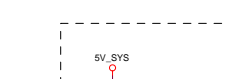
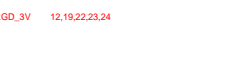
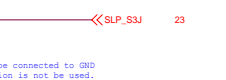
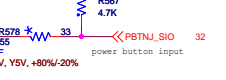
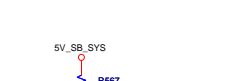
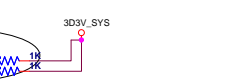
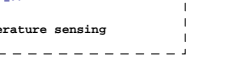
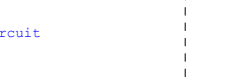
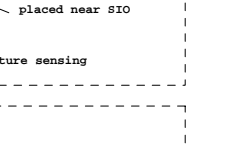
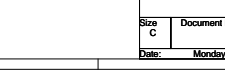
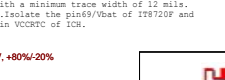
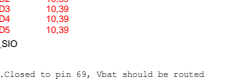
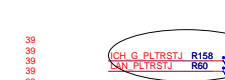
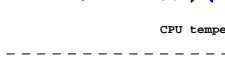
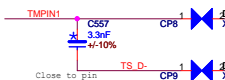
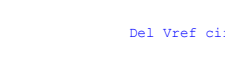
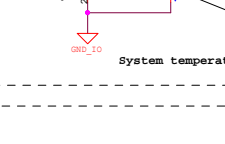
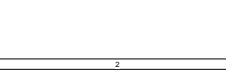
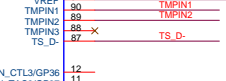
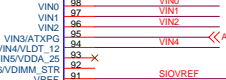
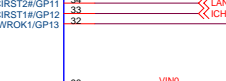
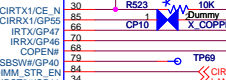
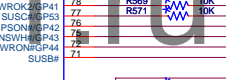
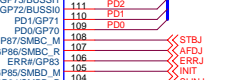
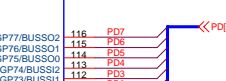
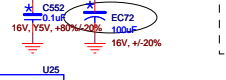
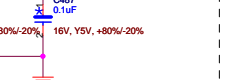
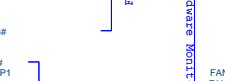
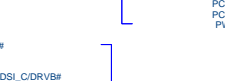
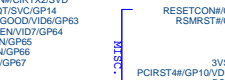
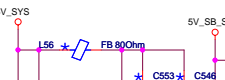
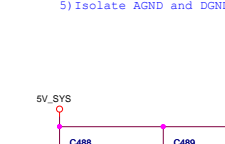
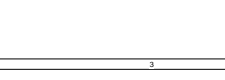
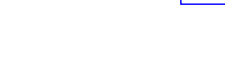
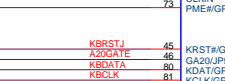
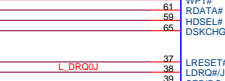
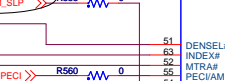
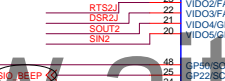
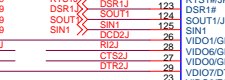
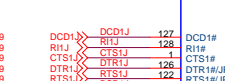
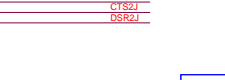
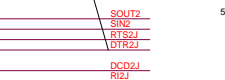
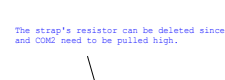
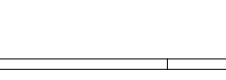
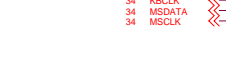
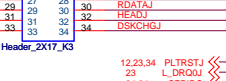
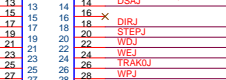
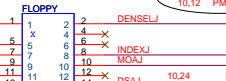
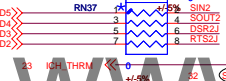
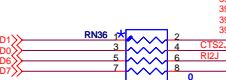
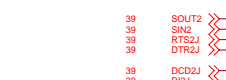
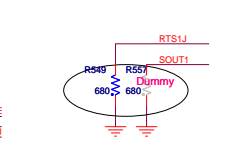
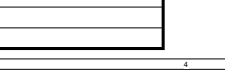
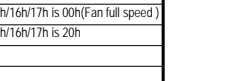
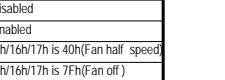
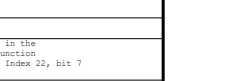
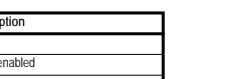
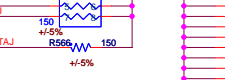
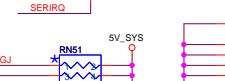
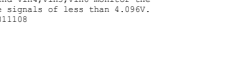
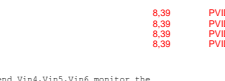
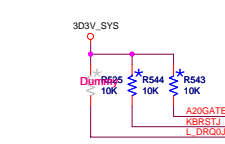


Note: Recommend Vin4, Vin5, Vin6 monitor the voltage signals of less than 4.096V.
Qty 011108

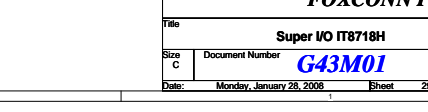
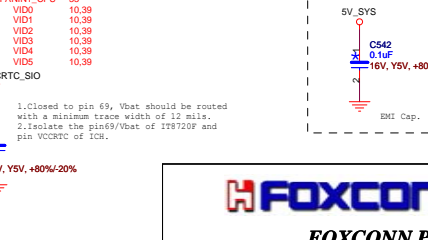
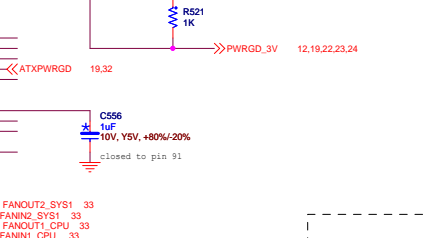
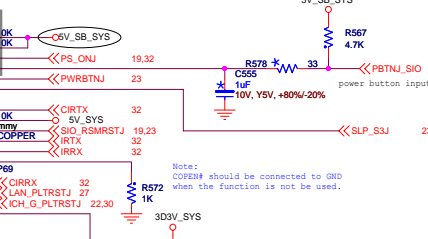
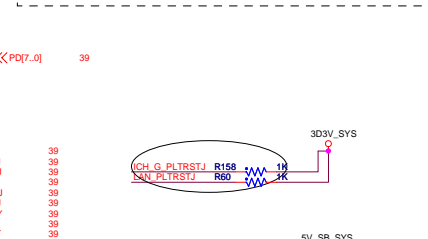
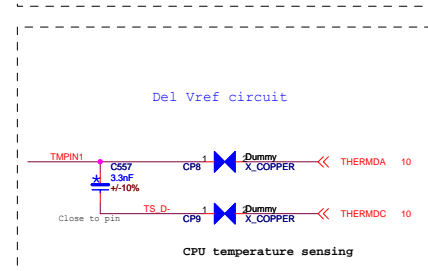
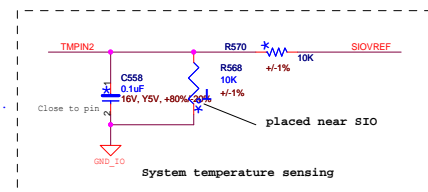


IT8720 Power On Strapping Options

Symbol	value	Description
JP1	Flashseg1_EN	1 Disabled.
JP2	VIDO_EN	0 Flash I/F Address Segment 1 is enabled
Pin 122	VIDO_EN	1 Disable VID output pins
Pin 124	CHIP_SEL	0 Enable VID output pins
JP4	K8PWR_EN	Use for chip 1 when two IT8718F exit in the same system. Chip is selected in conjunction with Global Configuration Register - Index 22, bit 7
Pin 126	K8PWR_EN	1 K8 power sequence function is disabled
		0 K8 power sequence function is enabled
JP3 & JP5	FAN_CTL_SEL	11 The default value of EC Index 15h/16h/17h is 40h(Fan half speed)
Pin 124 & 46		10 The default value of EC Index 15h/16h/17h is 7Fh(Fan off)
		01 The default value of EC Index 15h/16h/17h is 00h(Fan full speed)
		00 The default value of EC Index 15h/16h/17h is 20h
JP5	WDT_EN	1 Disable WDT to rest PWROK
Pin46		0 Enable WDT to rest PWROK
JP6	SVID_EN	1 Disable SVID Function
Pin29		0 Enable SVID Function



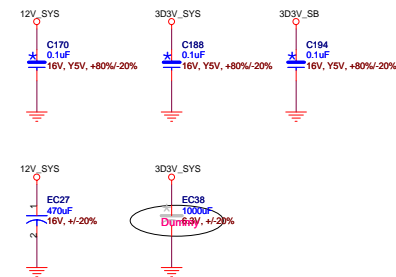
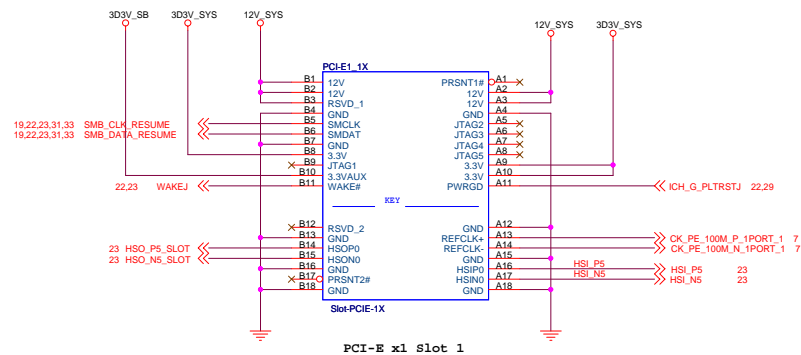
For the temperature sensor circuits,
1)Please don't remove the 1uF capacitor(C4) between Vref and AGND.
2)Place the thermal diode close to IT8720P.
3)Keep the trace away from +12V, fast data bus, and CRTs.
4)Recommended trace widths and spacings are 12 mils.
5)Isolate AGND and DGND.



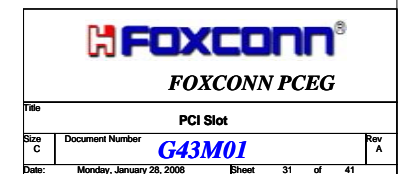
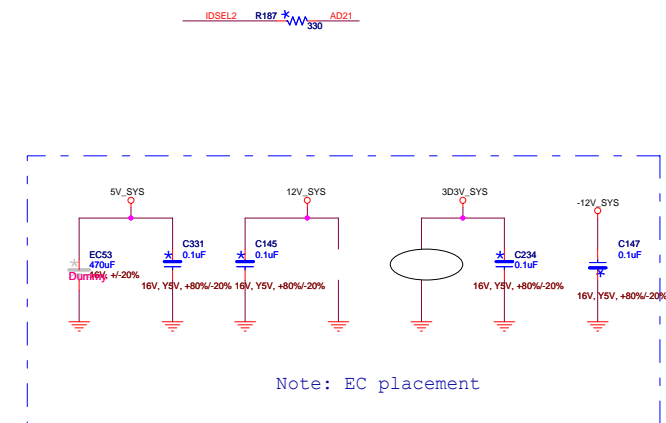
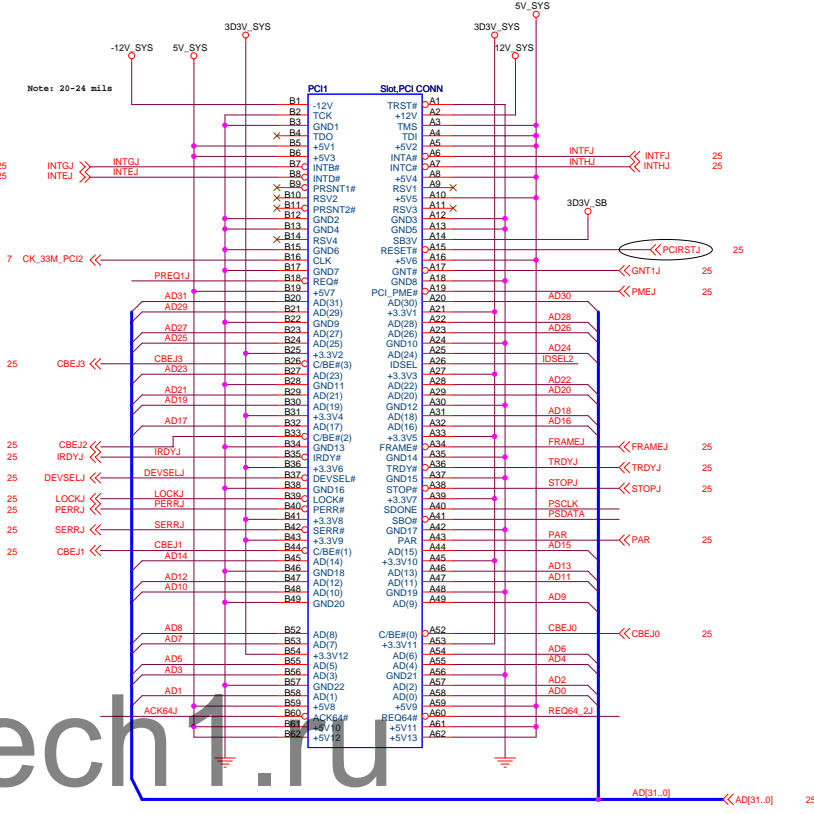
FOXCONN PCEG

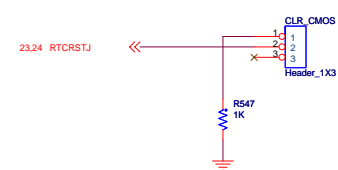
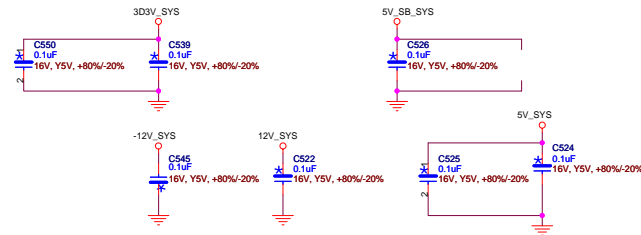
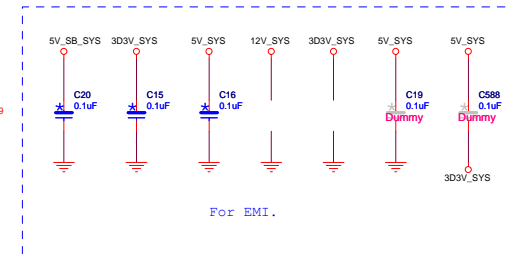
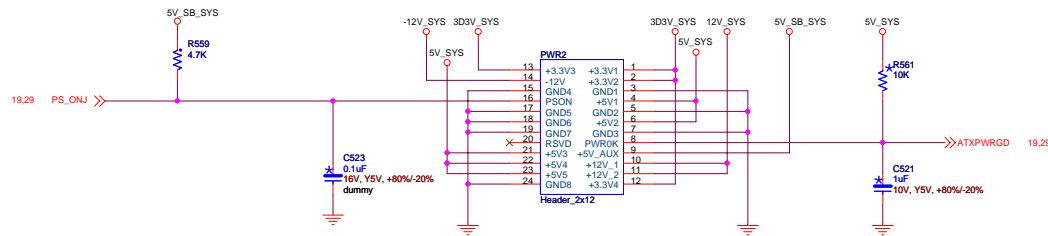
Super I/O IT8718H

File: 43M01
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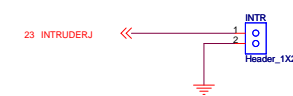


Clear CMOS

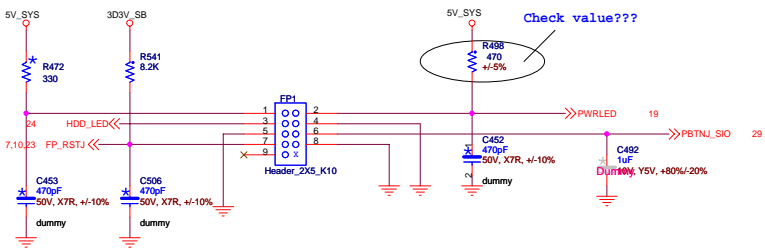
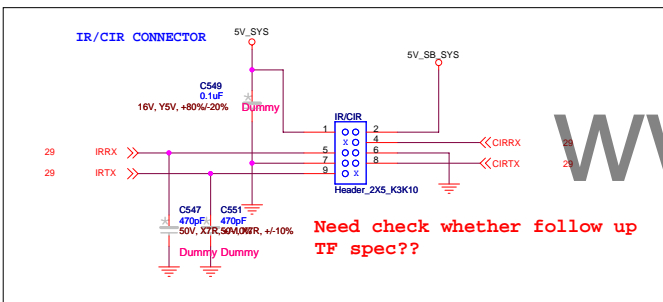
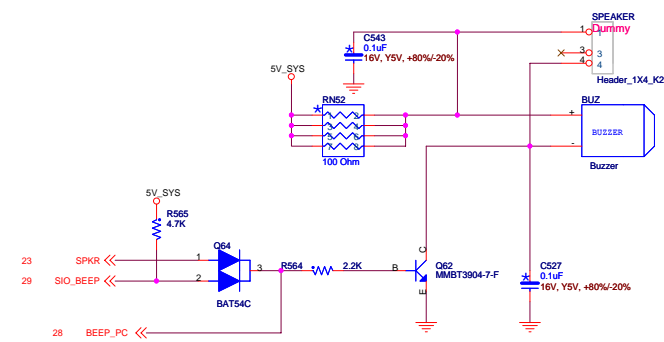
CLR_CMOS	CMOS
Clear	(1-2)
Normal	(2-3)

CLR_CMOS(2-3)
Jumper_2P_Blu

Chassis Intruder Header



SPEAKER HEADER

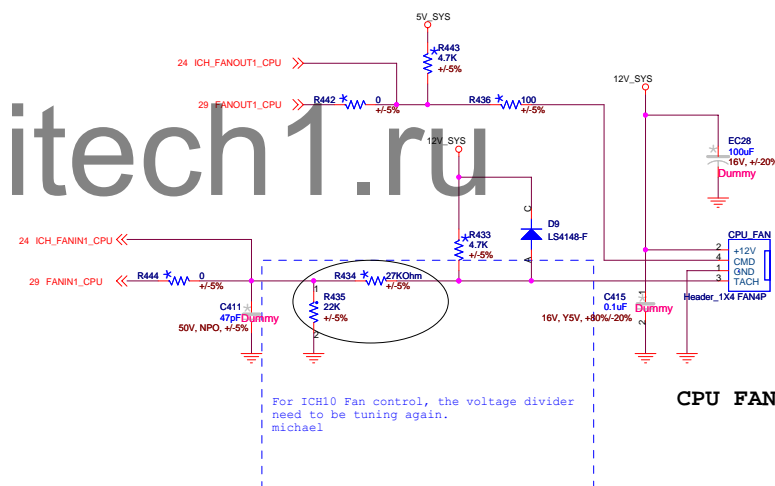
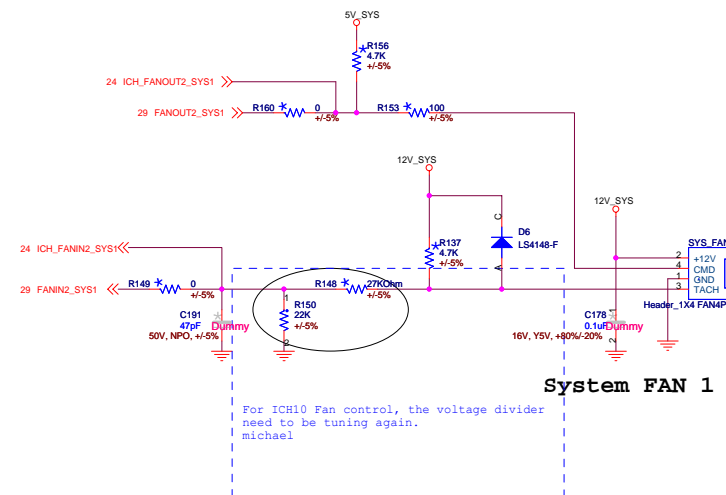
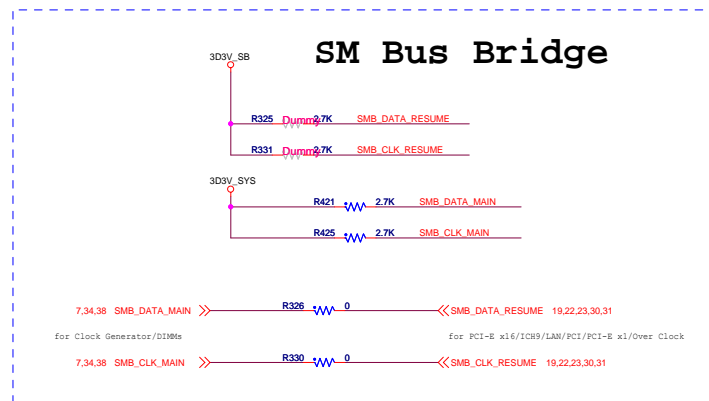


Front Panel Switch/LED

HDD_LED+	1	2	Power
HDD_LED-	3	4	Power LED (Green)
GND	5	6	Power button
Reset button	7	8	Power
NC	9	10	Key

FOXCONN PCEG

File		
ATX, FP, MISC Connector		
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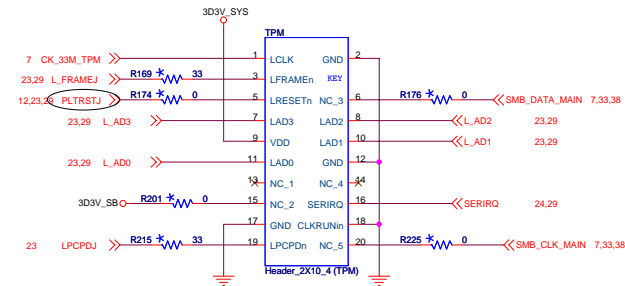
4-pin FAN Header Definition
pin1. GND
pin2. +12V
pin3. Sense
pin4. Control

Peak fan current draw: 1.5A
Average fan current draw: 1.1A
Fan start-up current draw: 2.2A
Fan start-up current draw maximum duration: 1.0 second
Fan header voltage: 12V +/- 10%

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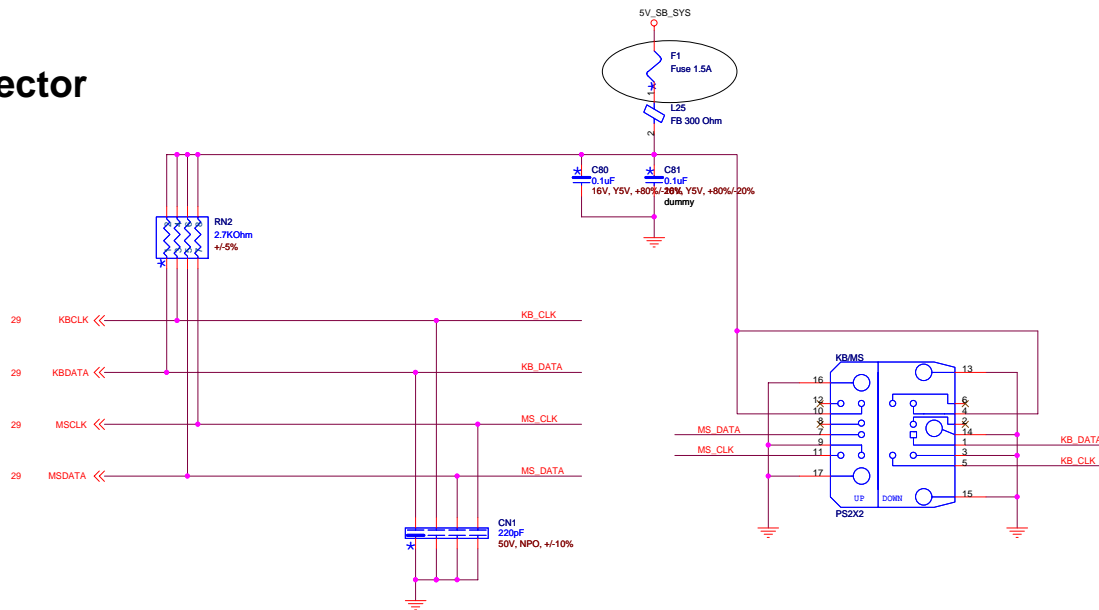
Del XDP Connector

TPM Connector

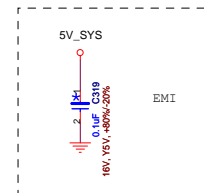
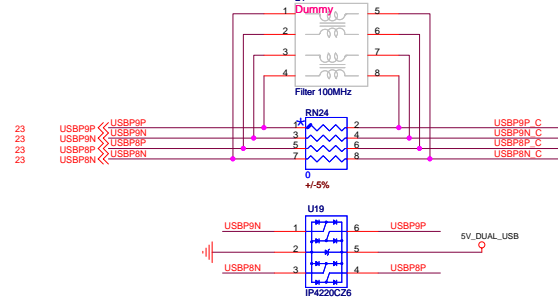
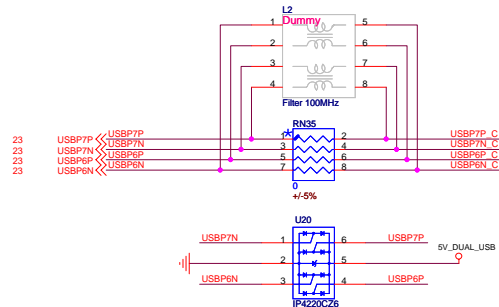
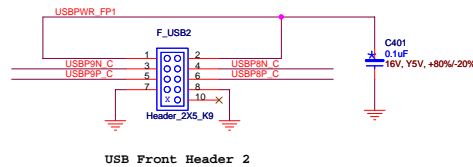
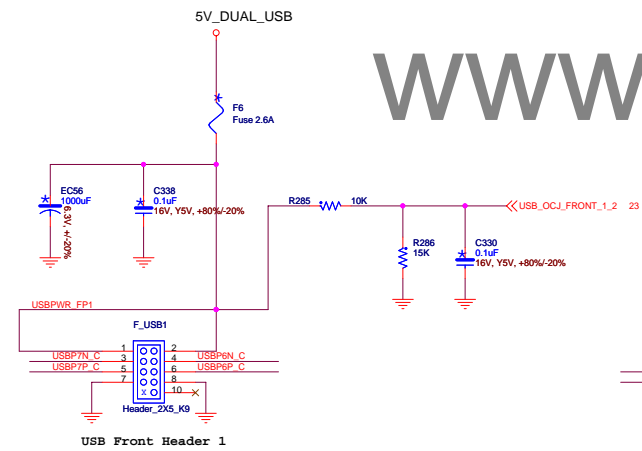
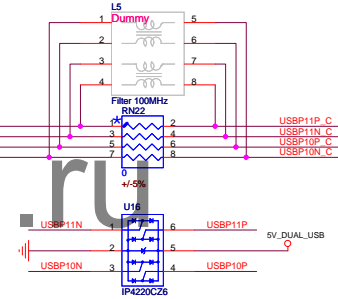
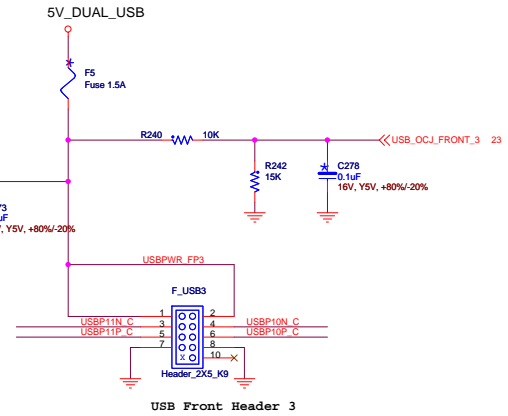


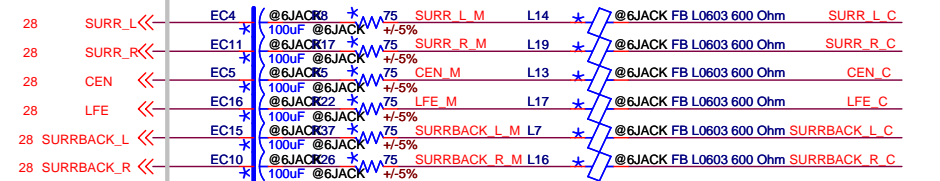
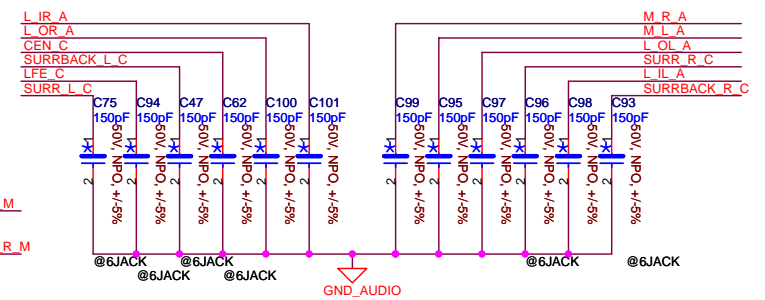
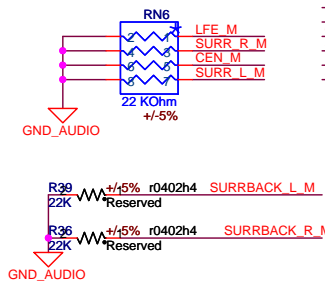
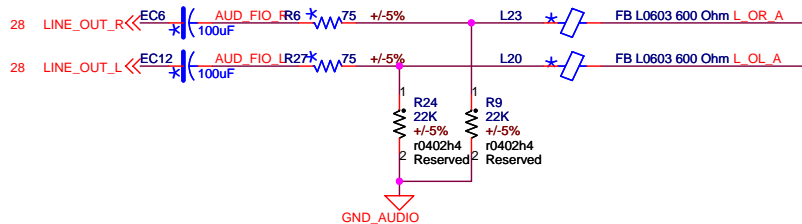
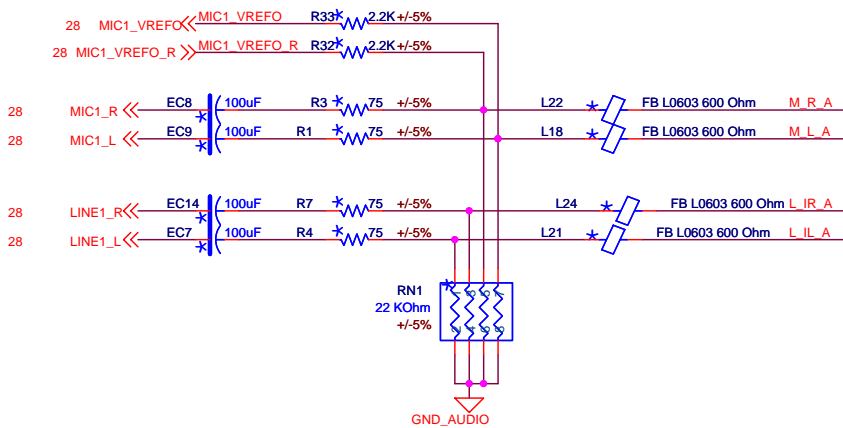
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KB / MS Connector

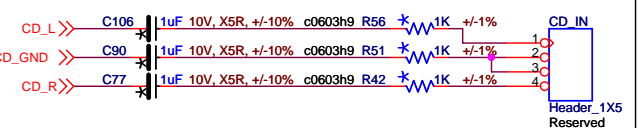
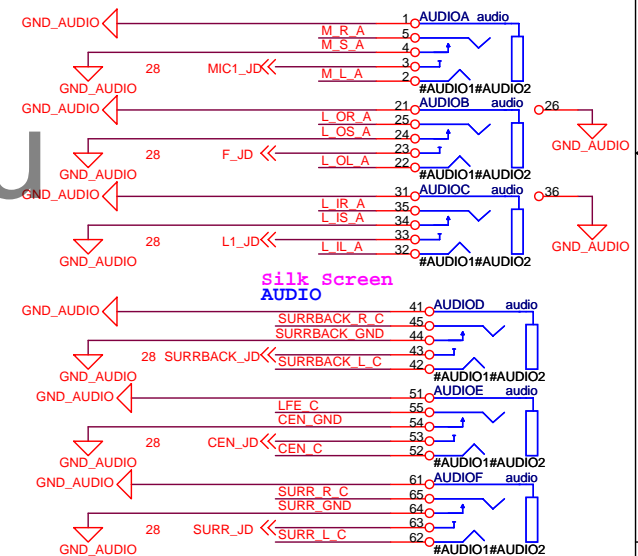
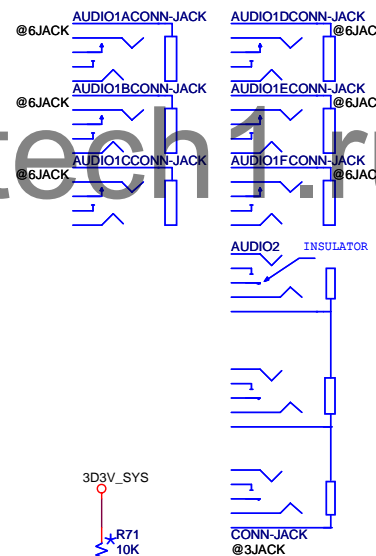
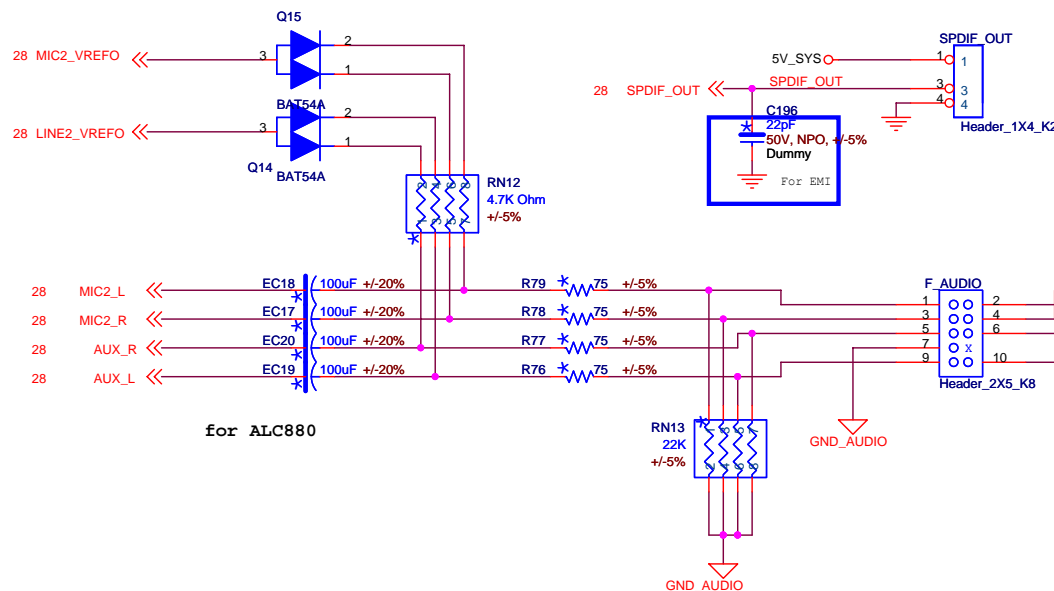



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Del F_USB header 4
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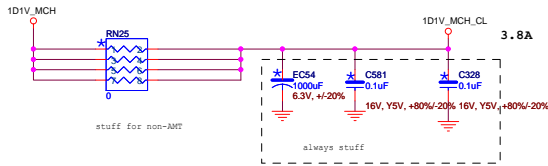


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Title			
HDA Audio Port			
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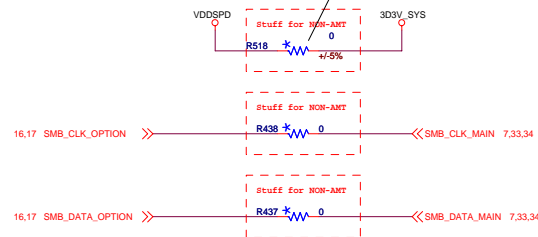
Del 1.1V MCH CL circuit
(1D8V_STR to 1D1V_MCH_CL)



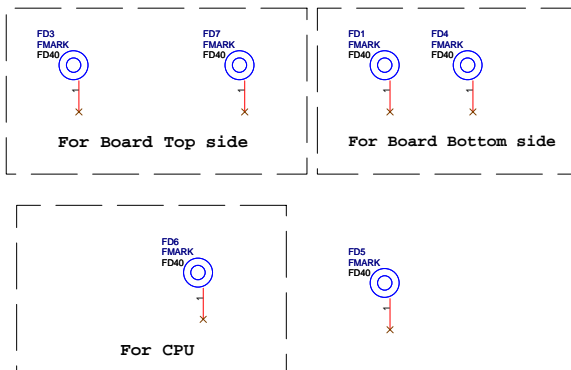
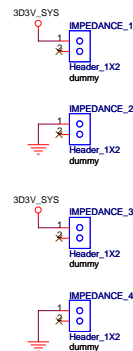
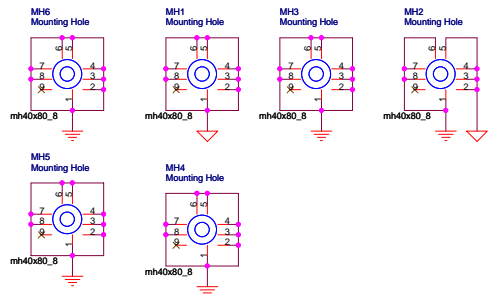
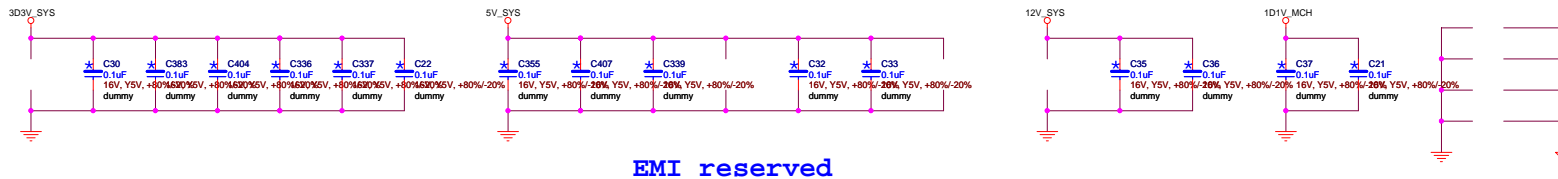
Del AMT Led circuit

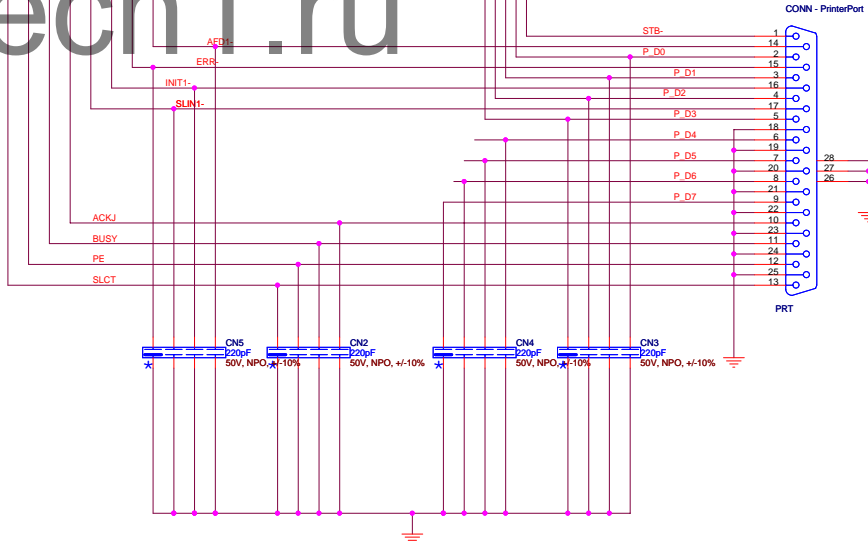
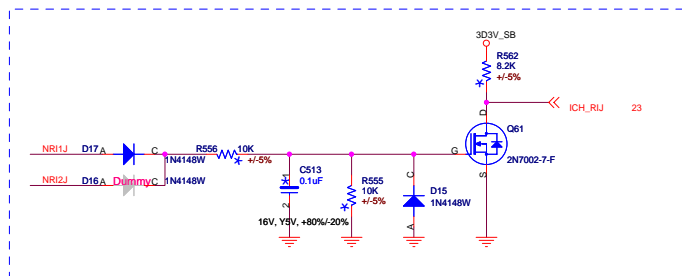
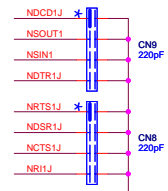
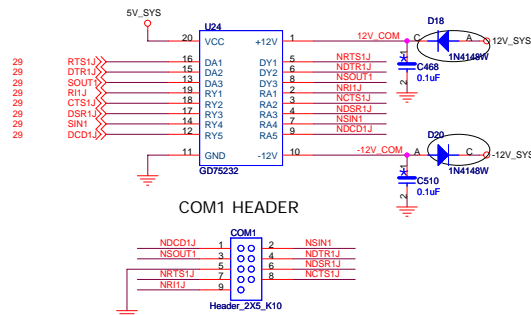
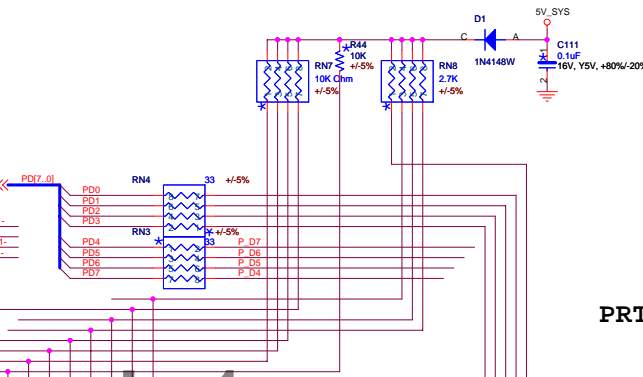
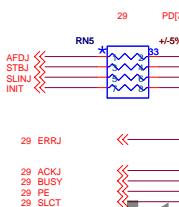
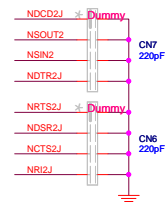
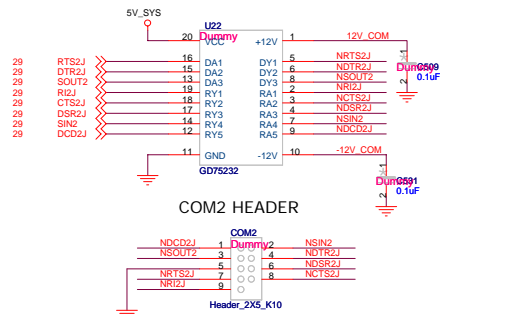
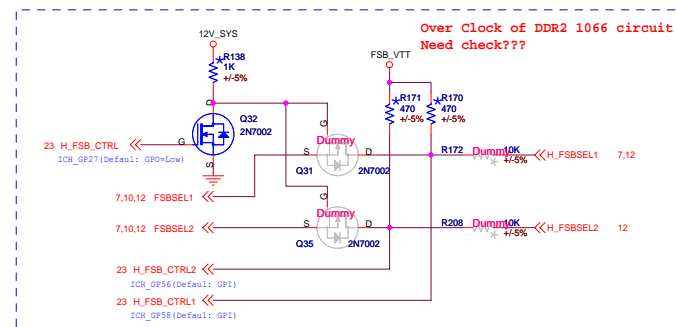
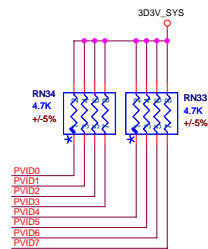
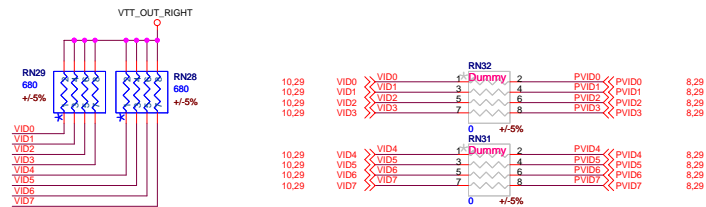
Del CL PWROK GENERATION

Change footprint to 0603



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ICH10 GPIO Summary

Name	Power Well	Type	Description
GPIO0	3.3V	I/O	FP_AUD_DETECT
GPIO1	3.3V	I/O	TACH_1
GPIO2	5V	I/OD	PIRQE#
GPIO3	5V	I/OD	PIRQF#
GPIO4	5V	I/OD	PIRQG#
GPIO5	5V	I/OD	PIRQH#
GPIO6	3.3V	I/O	TACH_2
GPIO7	3.3V	I/O	TACH_3
GPIO8	3.3V_SB	I/O	Unused(pull up)
GPIO9	3.3V_SB	I/O	WOL_ONLY
GPIO10	3.3V_SB	I/O	Unused(pull-up)
GPIO11	3.3V_SB	I/O	SMBALERT#
GPIO12	3.3V_SB	I/O	LAN_DISABLE#
GPIO13	3.3V_SB	I/O	L_PME#
GPIO14	3.3V_SB	I/O	Unused(pull-up)
GPIO15	3.3V_SB	I/O	CK_PCI_STOP
GPIO16	3.3V	I/O	Unused(NC)
GPIO17	3.3V	I/O	TACH_0
GPIO18	3.3V	I/O	Unused(NC)
GPIO19	3.3V	I/O	SATA_1GP
GPIO20	3.3V	I/O	Unused(NC)
GPIO21	3.3V	I/O	SATA_0GP
GPIO22	3.3V	I/O	Unused(pull-up)
GPIO23	3.3V	I/O	LDRQ1#
GPIO24	3.3V_SB	I/O	AMT_LED
GPIO25	3.3V_SB	I/O	CK_CPU_STOP
GPIO26	3.3V_SB	I/O	S4_STATE#
GPIO27	3.3V_SB	I/O	QRT_STATE0
GPIO28	3.3V_SB	I/O	QRT_STATE1
GPIO29	3.3V_SB	I/O	USB_OC3_FRONT#
GPIO30	3.3V_SB	I/O	USB_OC4_FRONT#
GPIO31	3.3V_SB	I/O	USB_OC4_FRONT#
GPIO32	3.3V	I/O	Unused(NC)
GPIO33	3.3V	I/O	MFG
GPIO34	3.3V	I/O	Unused(NC)
GPIO35	3.3V	I/O	Unused(NC)
GPIO36	3.3V	I/O	SATA_2GP
GPIO37	3.3V	I/O	SATA_3GP
GPIO38	3.3V	I/O	Unused(pull-up)
GPIO39	3.3V	I/O	Unused(pull-down)
GPIO40	3.3V_SB	I/O	USB_OC1_FRONT#
GPIO41	3.3V_SB	I/O	USB_OC2_FRONT#
GPIO42	3.3V_SB	I/O	USB_OC2_FRONT#
GPIO43	3.3V_SB	I/O	USB_OC3_FRONT#
GPIO44	3.3V_SB	N/A	USB_OC_BACK#
GPIO45	3.3V_SB	N/A	USB_OC_BACK#
GPIO46	3.3V_SB	N/A	USB_OC_BACK_LAN#
GPIO47	3.3V_SB	N/A	USB_OC_BACK_LAN#
GPIO48	3.3V	I/O	Unused(pull-up)
GPIO49	3.3V	I/O	DMI_STRAP(pull-down)
GPIO50	5.5V	I/O	REQ_1#
GPIO51	3.3V	I/O	Unused(NC)
GPIO52	5.5V	I/O	REQ_2#
GPIO53	3.3V	I/O	Unused(NC)
GPIO54	5.5V	I/O	REQ_3#
GPIO55	3.3V	I/O	Unused(NC)
GPIO56	3.3V_SB	I/O	Unused(pull-up)
GPIO57	3.3V_SB	I/O	Unused(pull-up)
GPIO58	3.3V_SB	I/O	Unused(pull-up)
GPIO59	3.3V_SB	I/O	USB_OC1_FRONT#
GPIO60	3.3V_SB	I/O	Unused(pull-up)

PCI Routing Summary


	PCI1				
INTAJ	F				
INTBJ	G				
INTCJ	H				
INTDJ	E				
INTEJ					
INTFJ					
INTGJ					
INTHJ					
REG#/GNT#	0				
IDSEL	16				

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ELM01-A_VPRO_1025->ELM01-A1_VPRO_1204.....2007/12/4 update

- 1)Add CK_PCI3_STRAP(pin5 of CK505) and modify CK_33M_80PORT_R(pin4 of CK505) for HW strapping (page7)
- 2)PR41 change to 2.8Kohm and PR30, PR37, PR47, PR52 change to 1.2Kohm for On-Semi fine-tune the solution of 05A (page8)
- 3)Change the circuit of PSI for Intel MSDW updated (page8)
- 4)Reserve the circuit of Auto-PSI for On-Semi updated (page8)
- 5)R109 change to dummy for Intel CRB updated (page10)
- 6)Stuff R346 and R342 for C3,C4 power management support (page12)
- 7)Change U4 to Intersil ISL6545CBZ-T for 1D1V_MCH core power updated (page19)
- 8)Stuff RN48, RN49, RN51 to short the FSB_VTT to 1D1V_MCH (page19)
- 9)Change the circuit of SDVO_CTRLCLK and SDVO_CTRLDATA for Intel CRB updated (page21)
- 10)Reserve 1X3 header of PEG_SEL for the PEG_PINB7 of ATI PCIE-Graphic card issue (page22)
- 11)Reserve the pin of PEG_PINB21 for the PEG_PINB7 of ATI PCIE-Graphic card issue (page22)
- 12)Stuff R343 and R344 for C3,C4 power management support (page23)
- 13)Reserve R502 and R652 for the co-layout circuit of IT8720F (ver:B and ver:C) (page29)
- 14)C436 connect to TS_D- and C435 connect to GND_IO (page29)

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File			
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